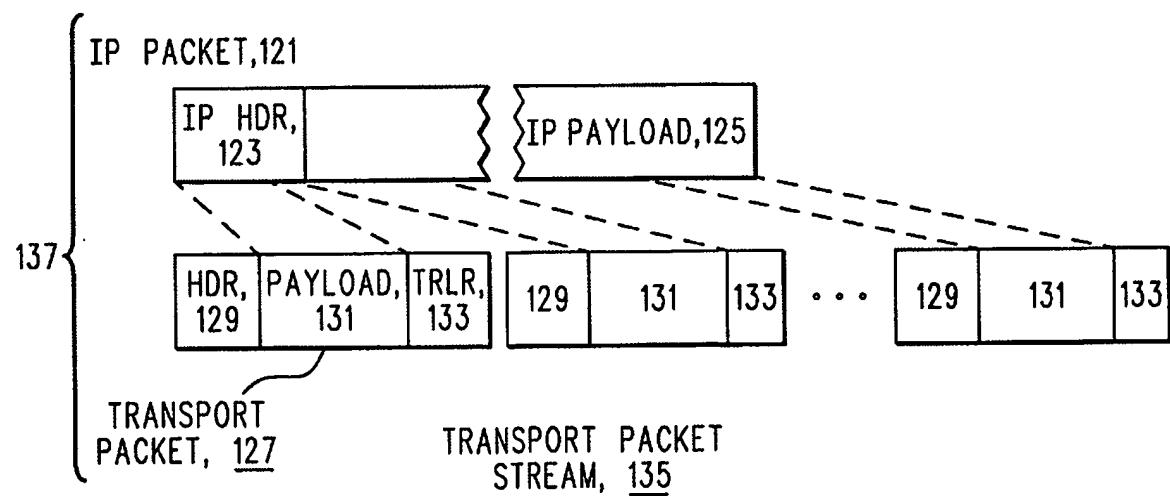


101



PACKET, 113



**Fig.1**  
(PRIOR ART)

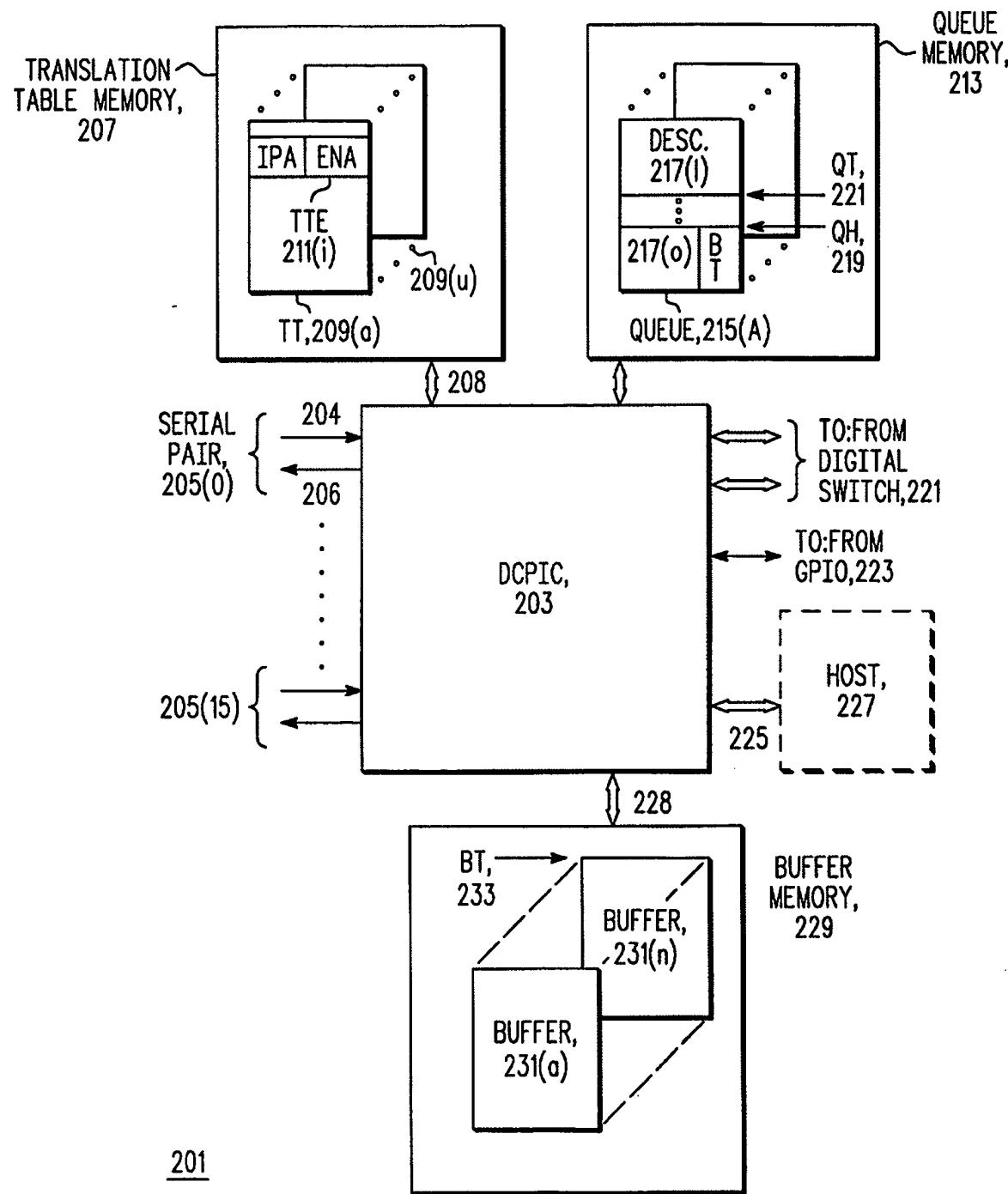
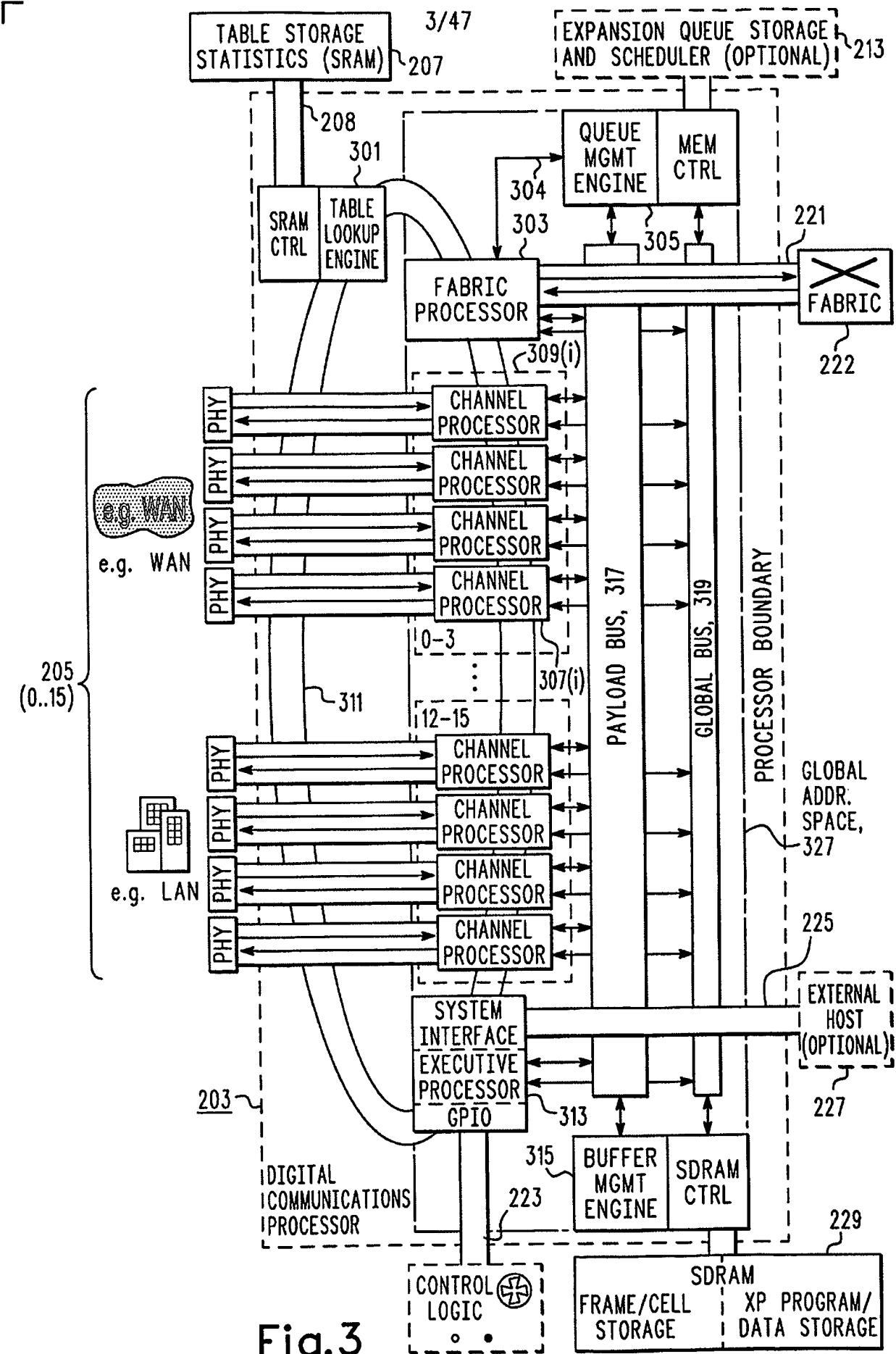


Fig.2

JUL 03 2006



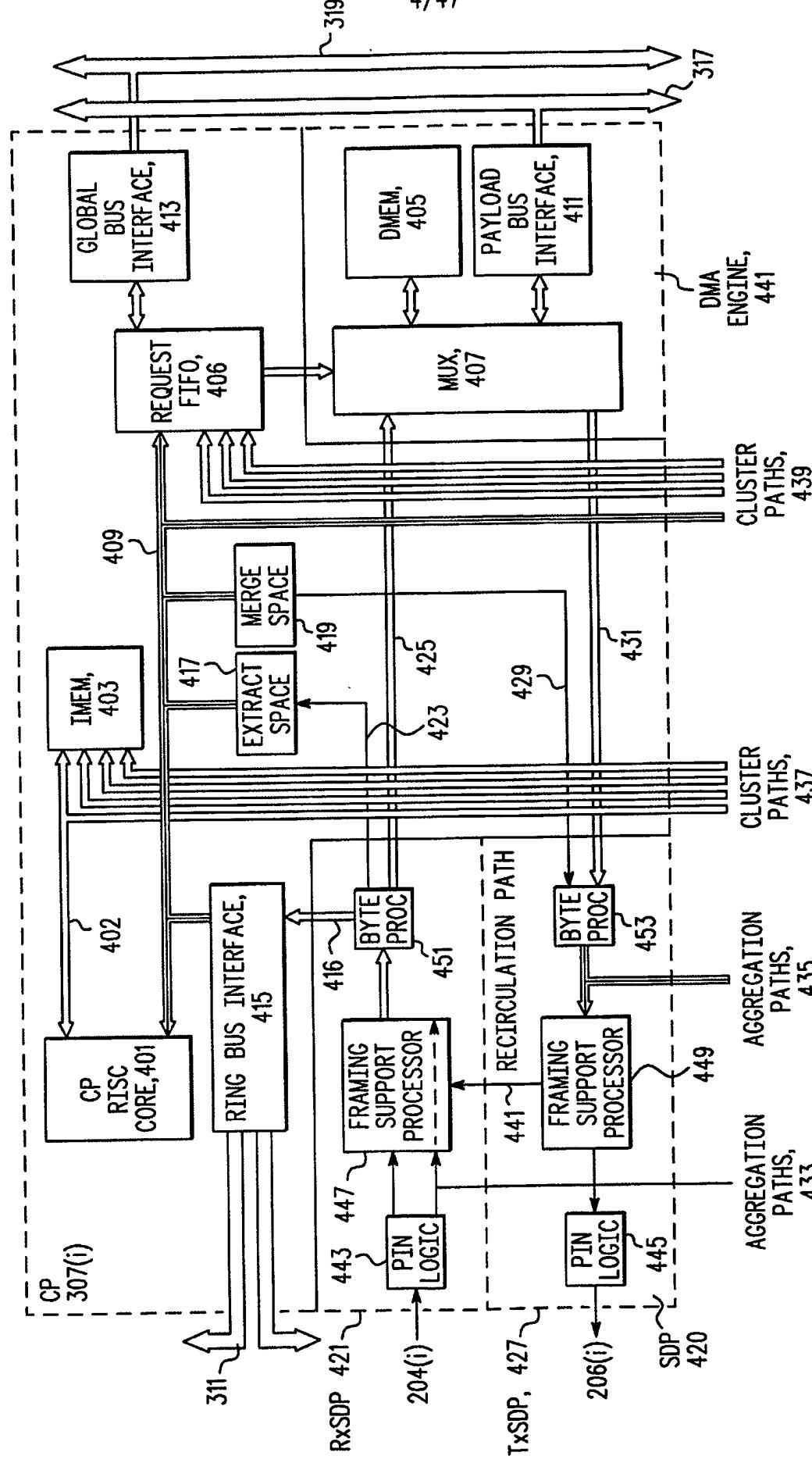
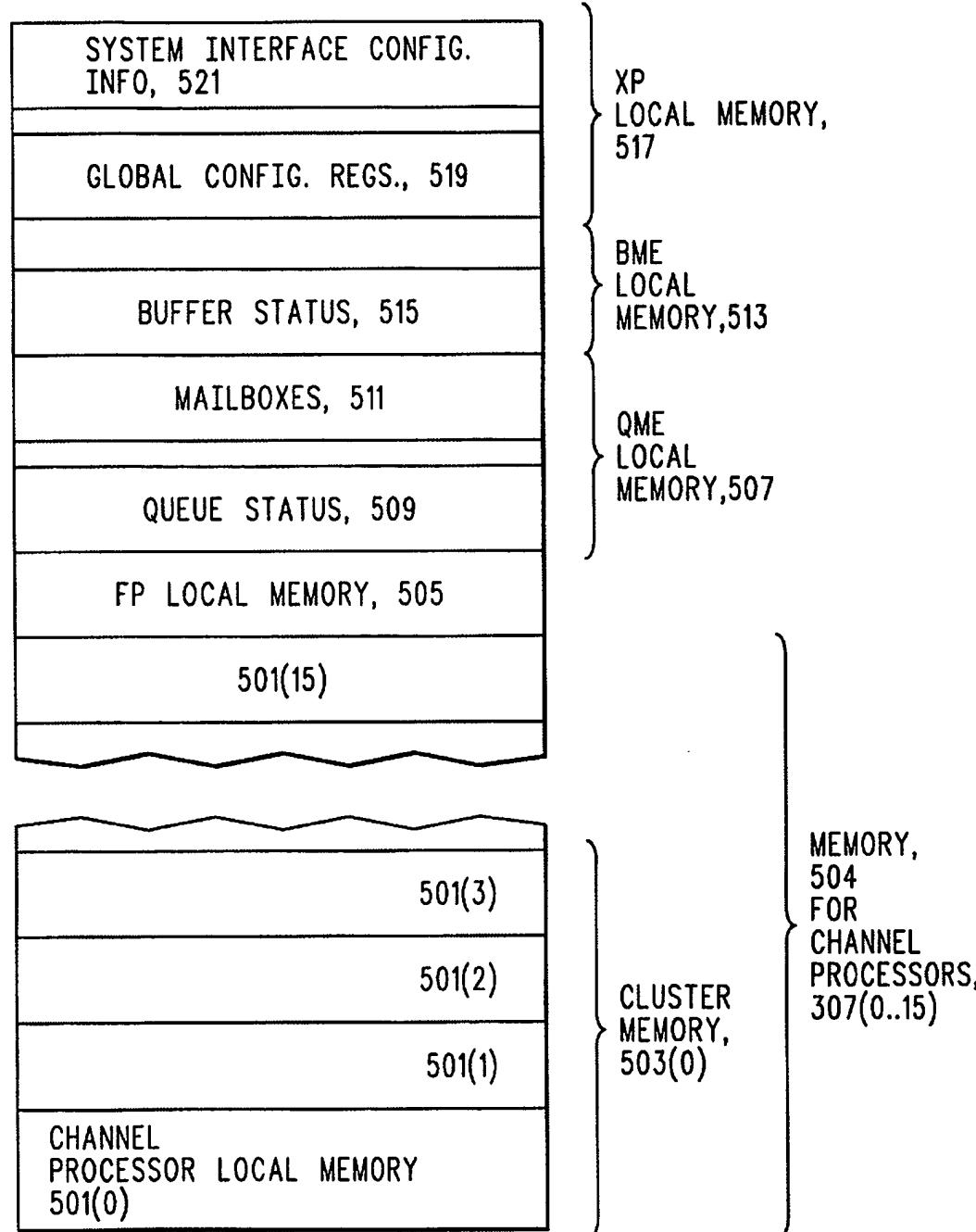
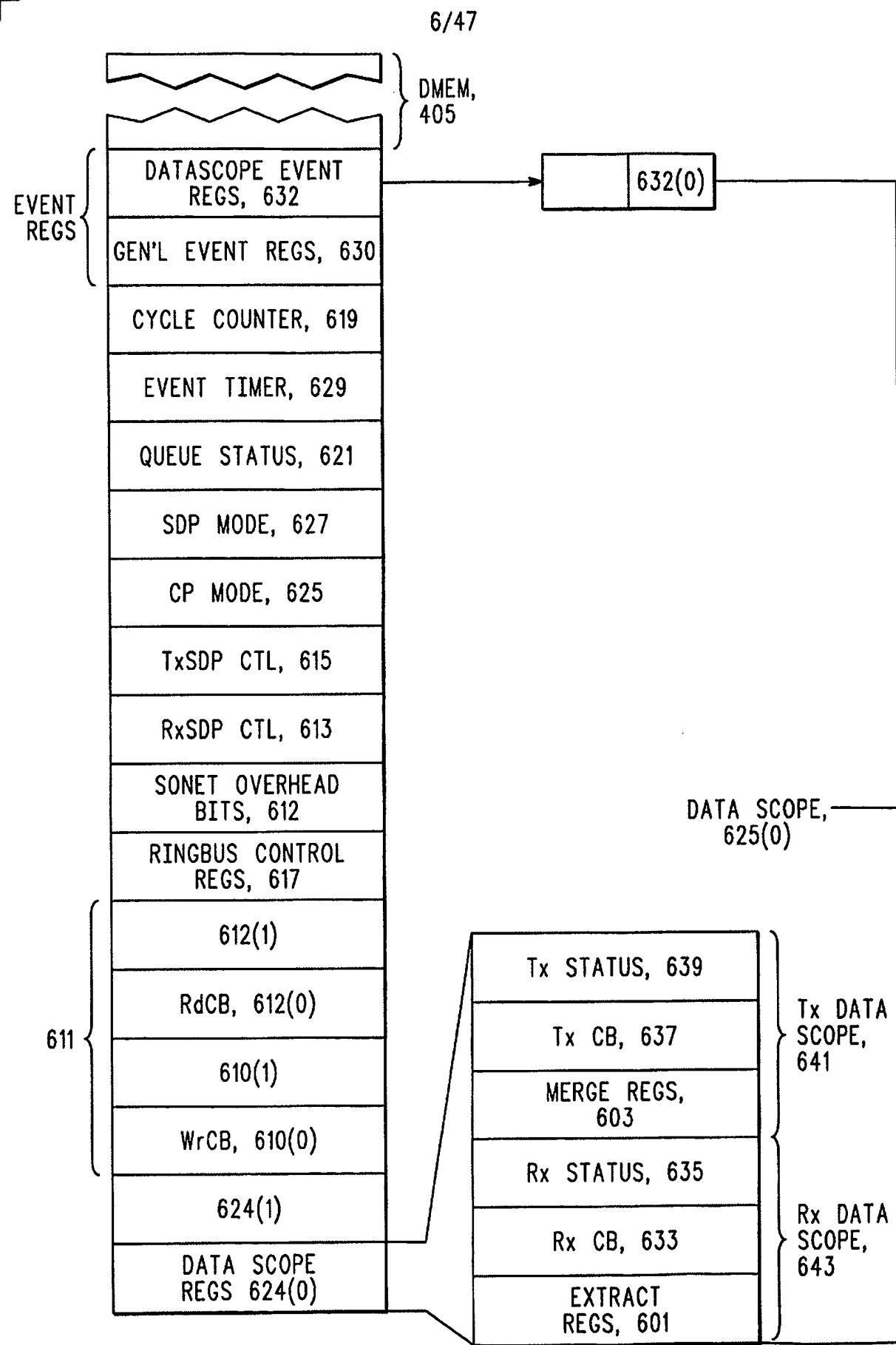


Fig.4





## Replacement Sheet

BRIGHTMAN ET AL.  
SC10981TS

601(i)

Fig.6



JUL 03 2006

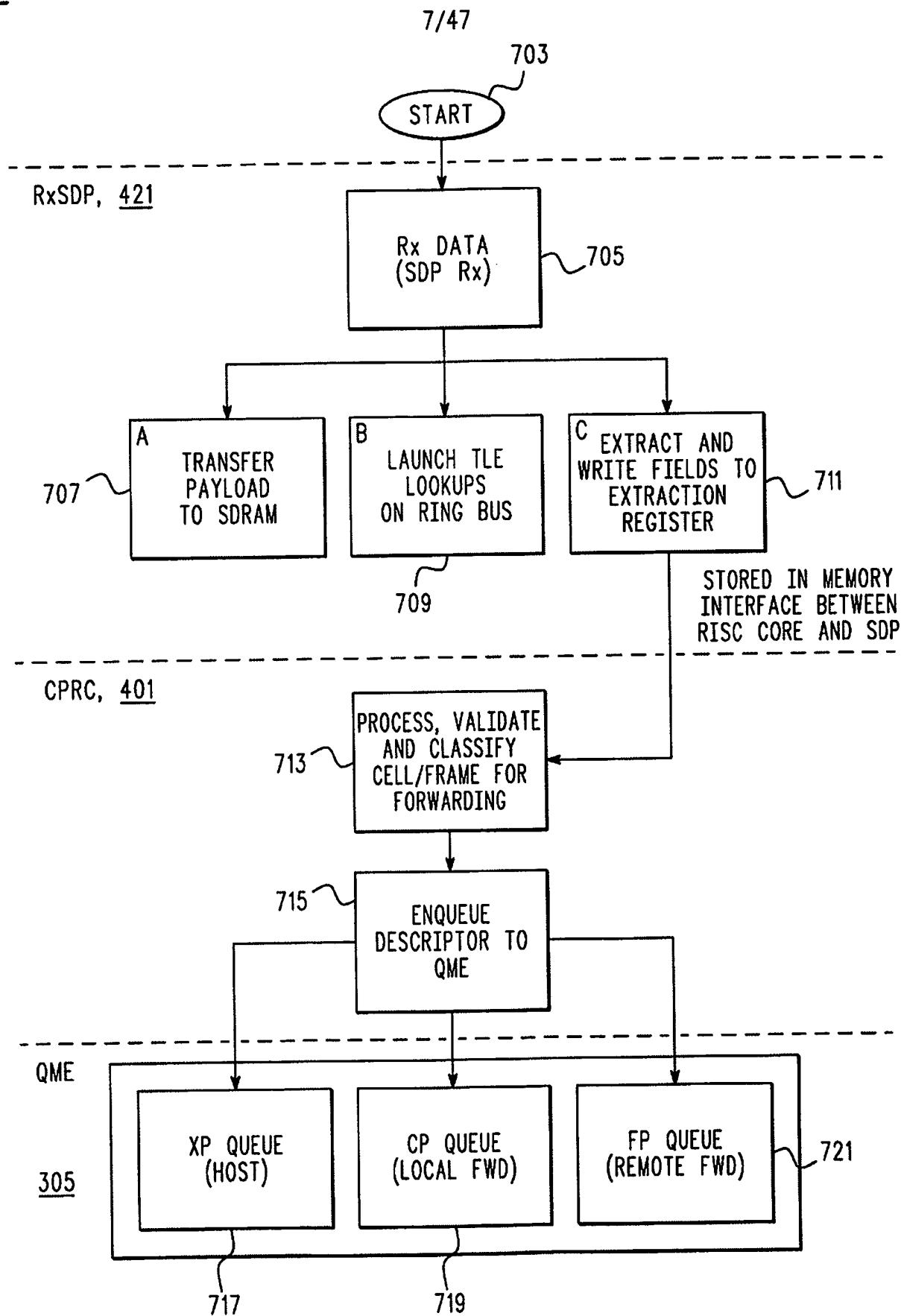


Fig.7

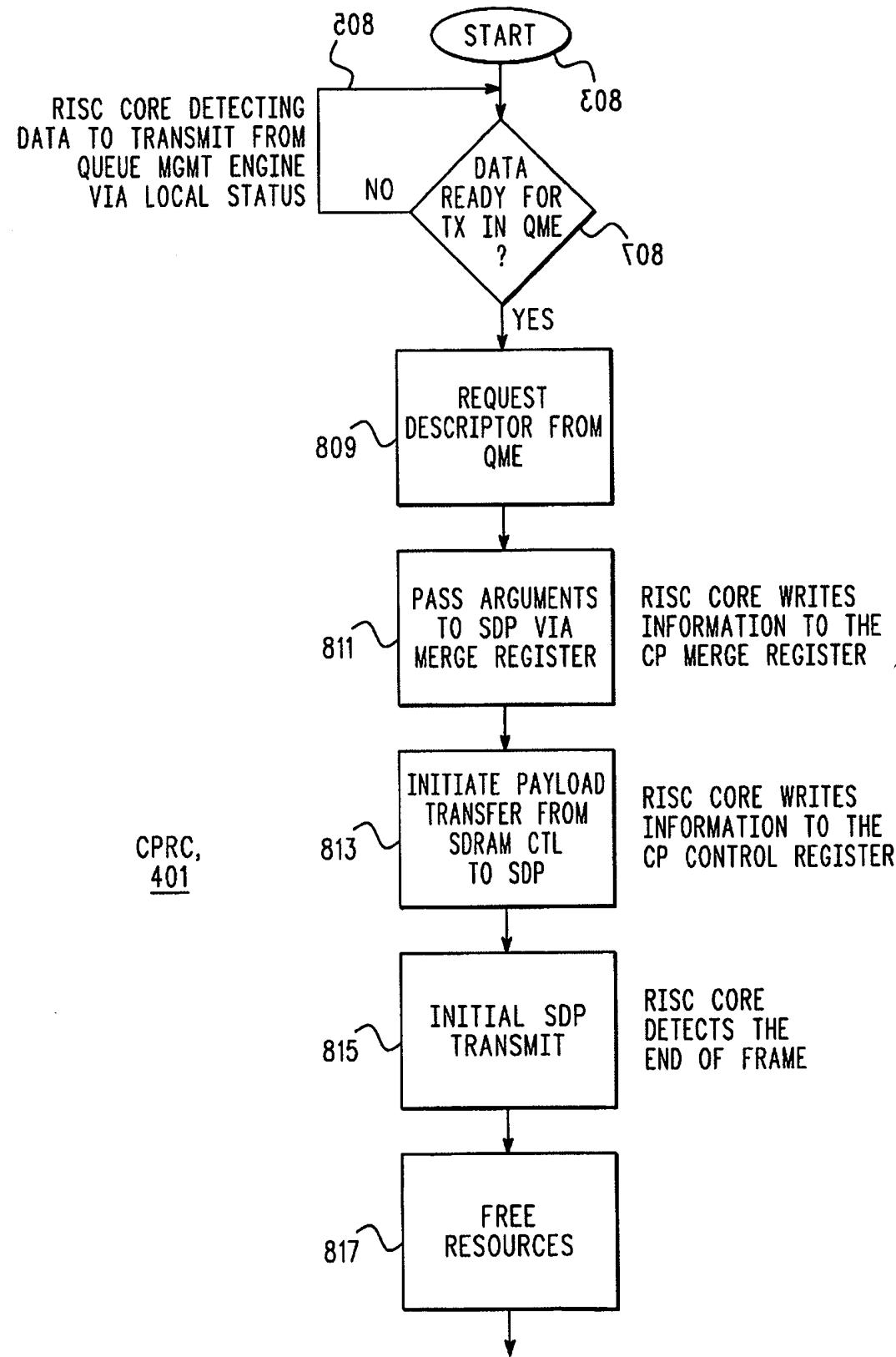


Fig.8



JUL 03 2006

9/47

OWN, 935	L5:L0 937	BUSY, 941
-------------	--------------	--------------

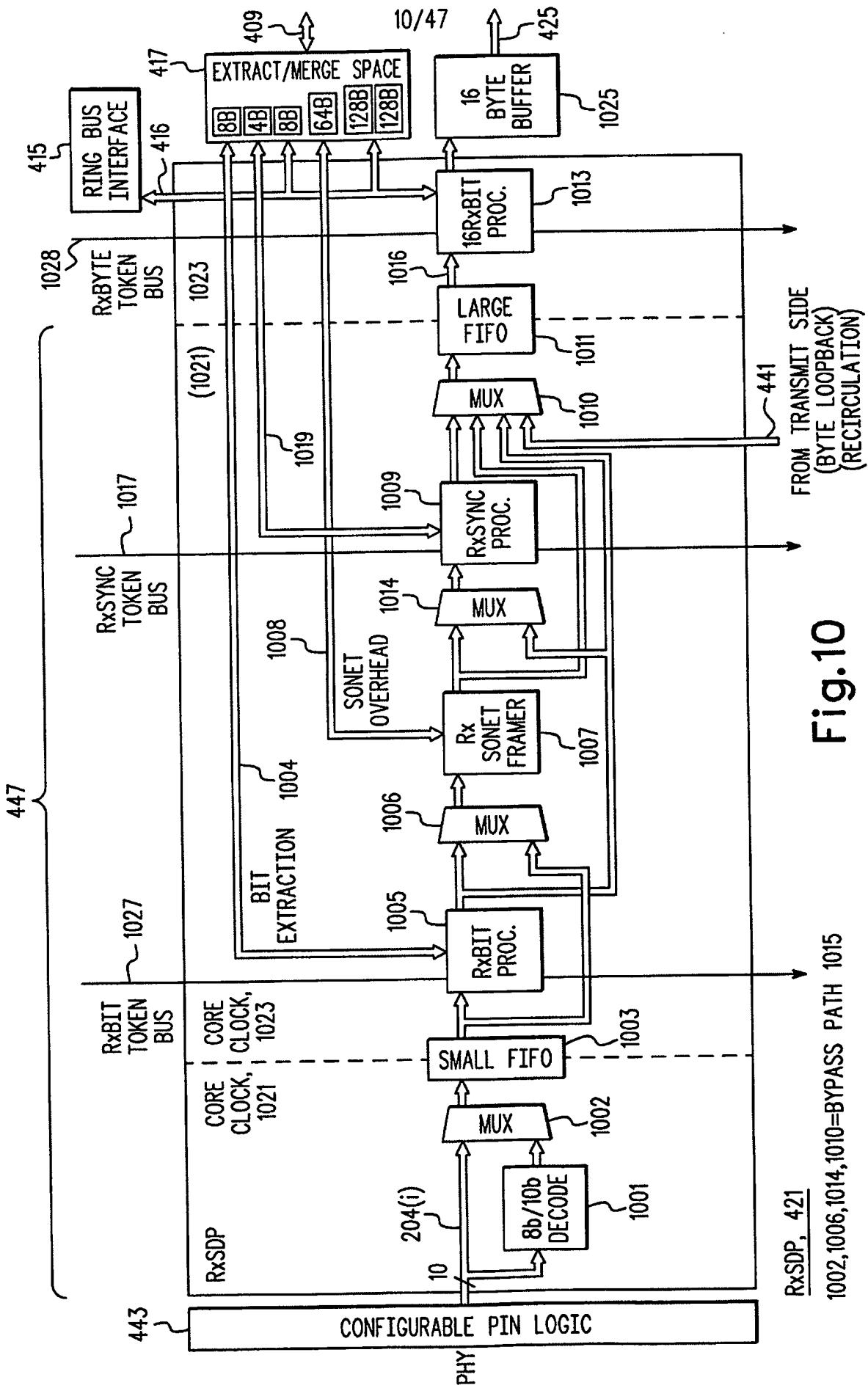
635

BTAG, 933			
OFFSET, 931			
Av, 929	NR, 927	Err, 925	OWN, 921
SDPST, 915	EOP, 927	BCTL, ST 919	
LENGTH, 911			
BUFFER POOL NO, 909			
DMEM DMAADDR, 907			
TxRcy ADDR., 905			
RxRcy ADDR., 903			
DMEM BYTE ADDR., 901			

{ RxCBCTL, 913

633

Fig.9

**Fig. 10**

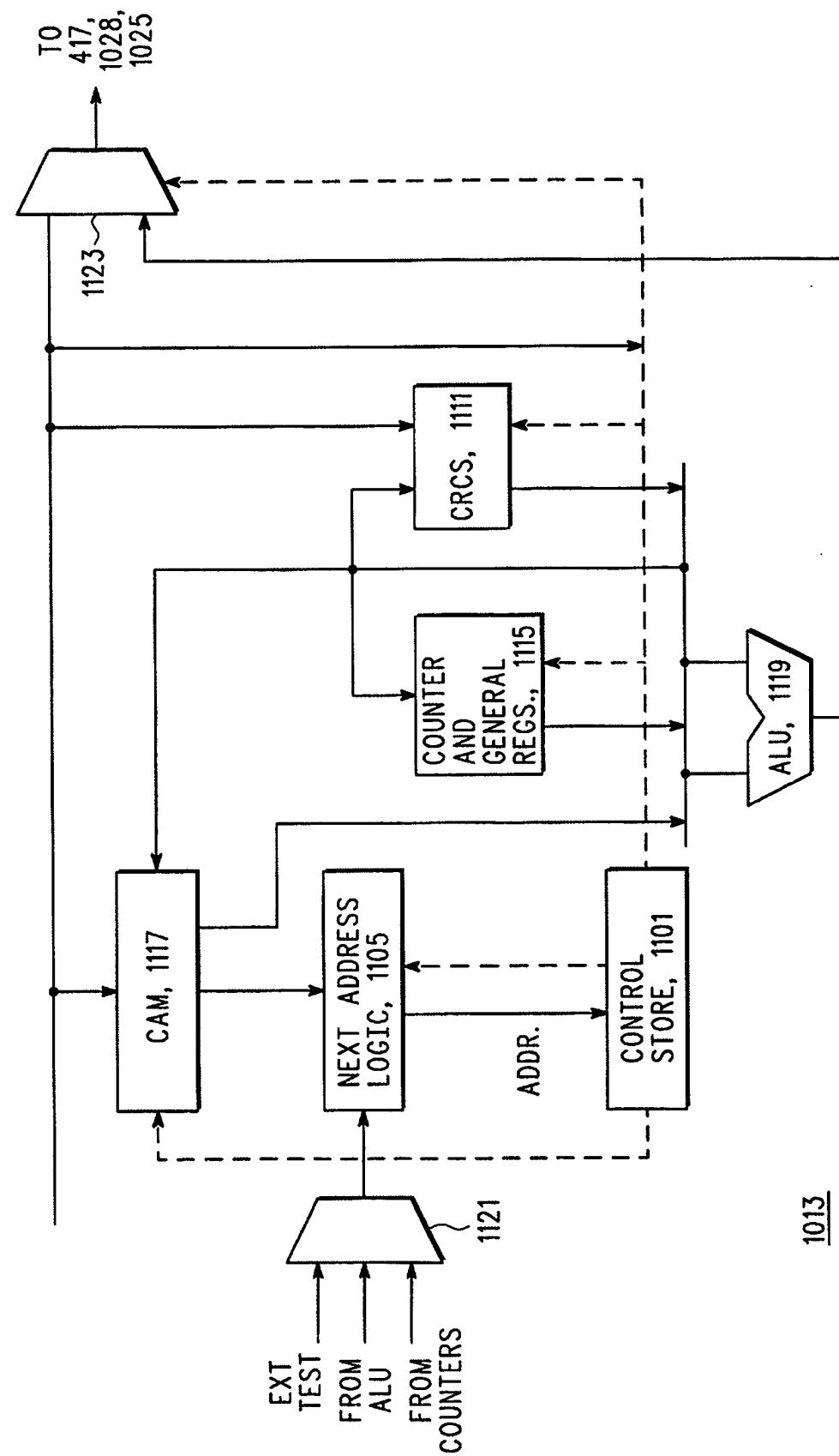
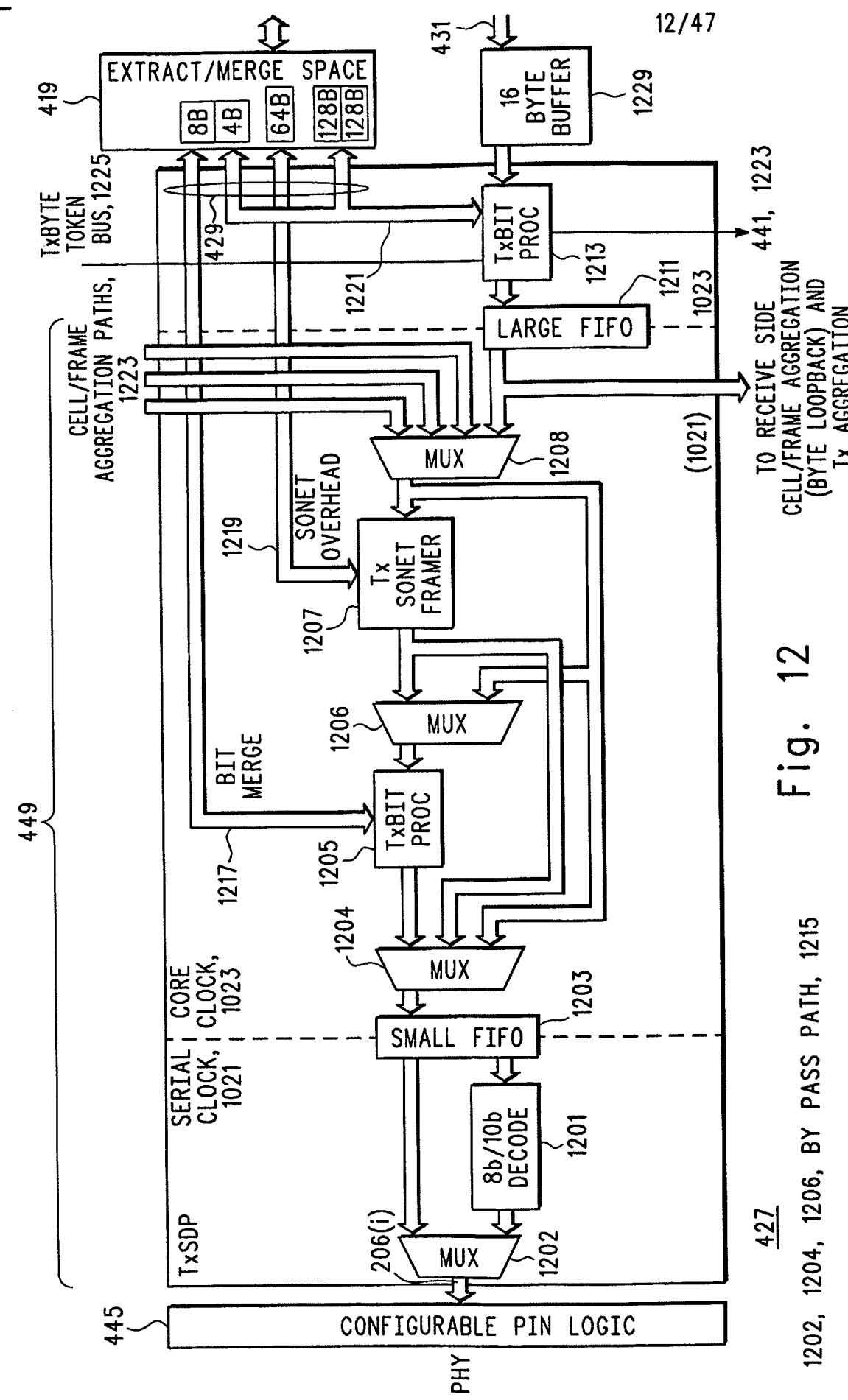


Fig. 11

1013



427

1202, 1204, 1206, BY PASS PATH, 1215  
1202, 1204, 1206, BY PASS PATH, 1215

Fig. 12

TO RECEIVE SIDE  
CELL/FRAME AGGREGATION  
(BYTE LOOPBACK) AND  
Tx AGGREGATION

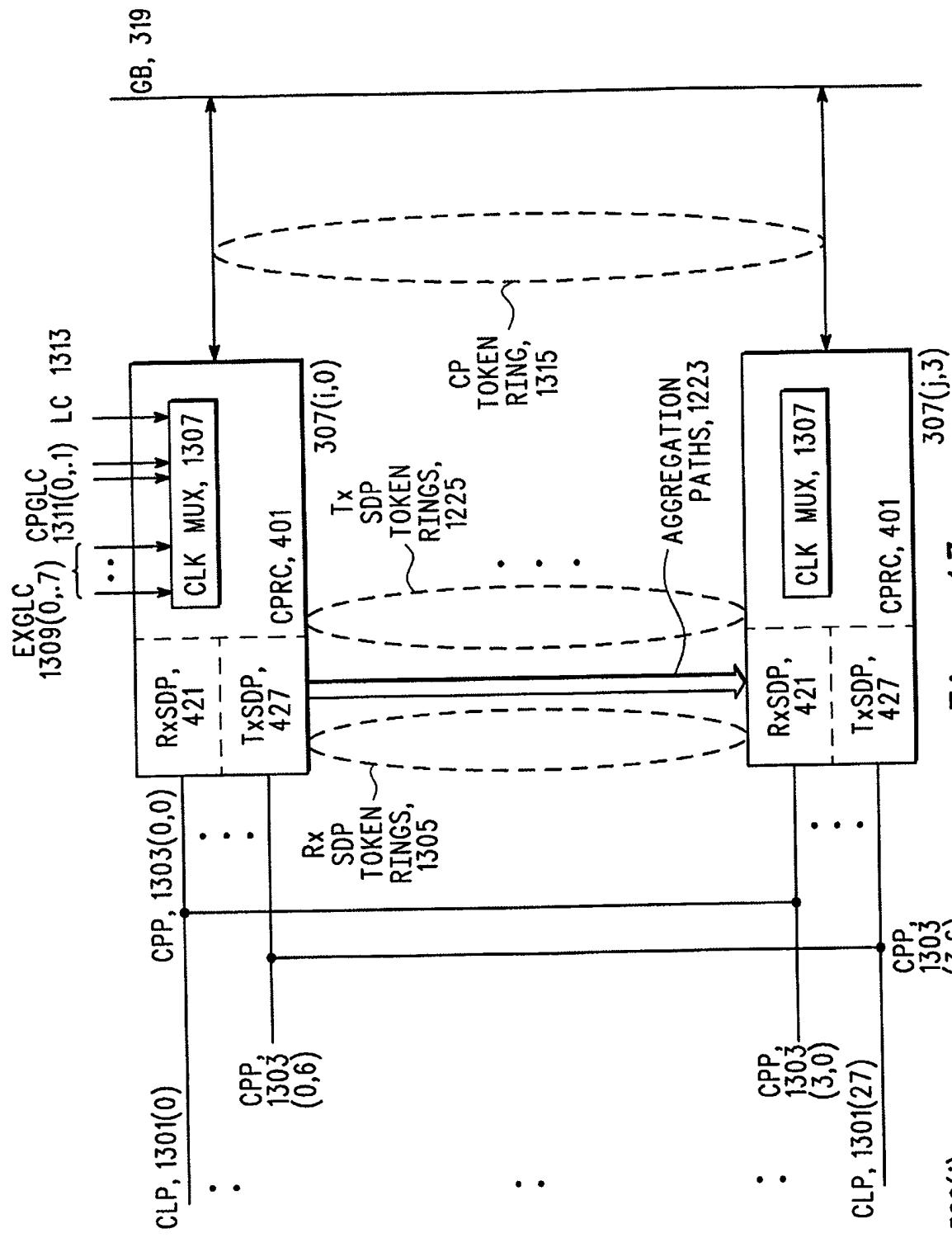
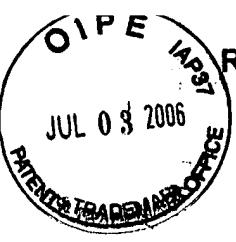


Fig. 13

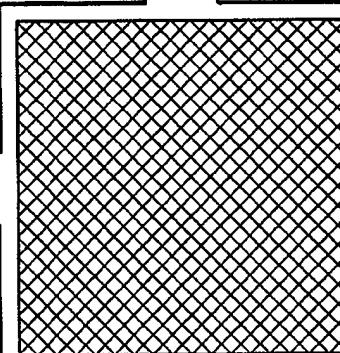
309(j)



MEM, 503(i,3)

SDP, 1403	DMEM, 405	BUS CONTROL, 1405
--------------	--------------	-------------------------

RISC CORE, 1407	IMEM, 403	
-----------------------	--------------	--



503(i,2)

BUS CONTROL	DMEM	SDP
----------------	------	-----

IMEM	RISC CORE
------	--------------

RISC CORE	IMEM
--------------	------

SDP	DMEM	BUS CONTROL
-----	------	----------------

IMEM	RISC CORE
------	--------------

BUS CONTROL	DMEM	SDP
----------------	------	-----

503(j,0)

509

503(j,1)

Fig. 14

L



15/47

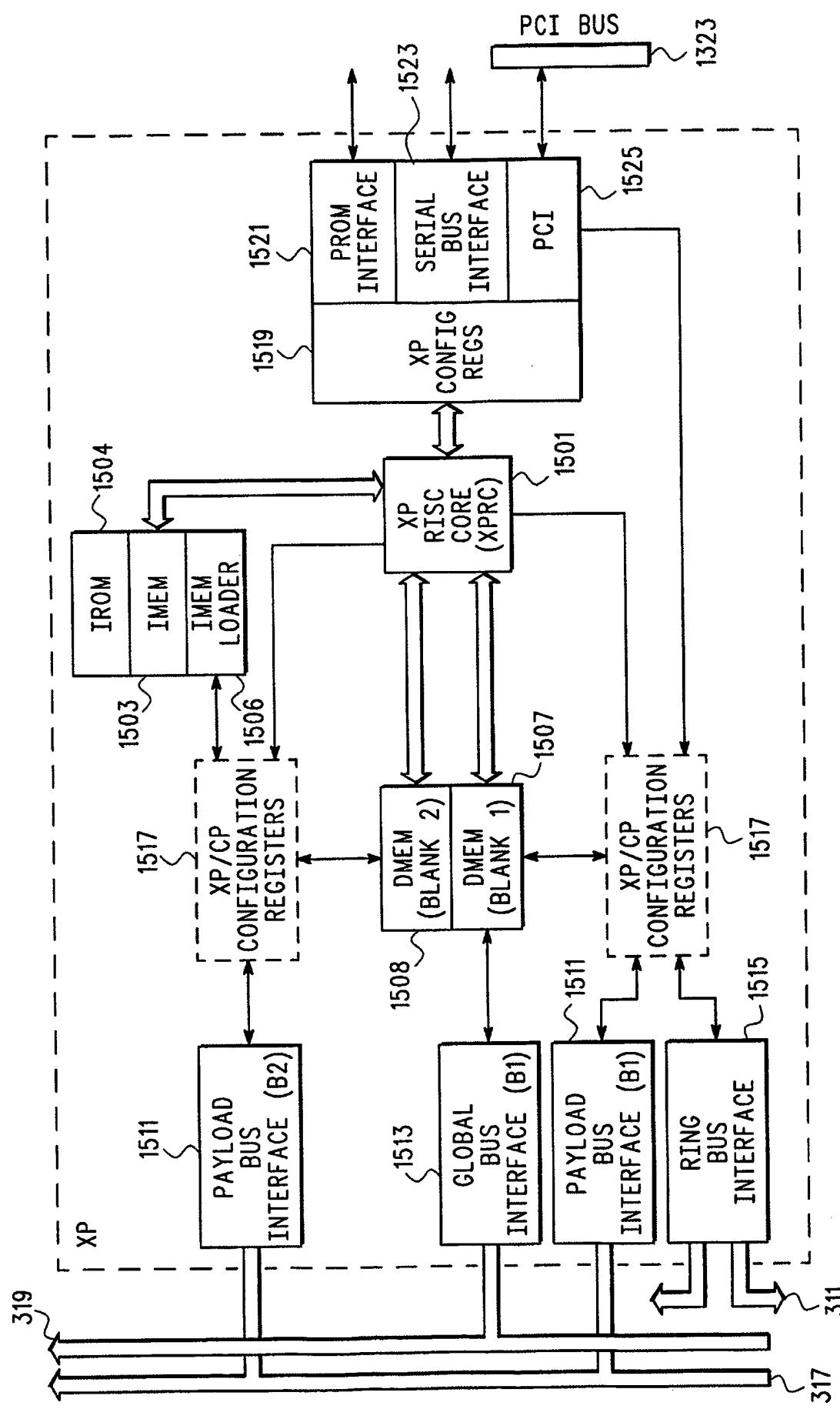


Fig. 15

317

311

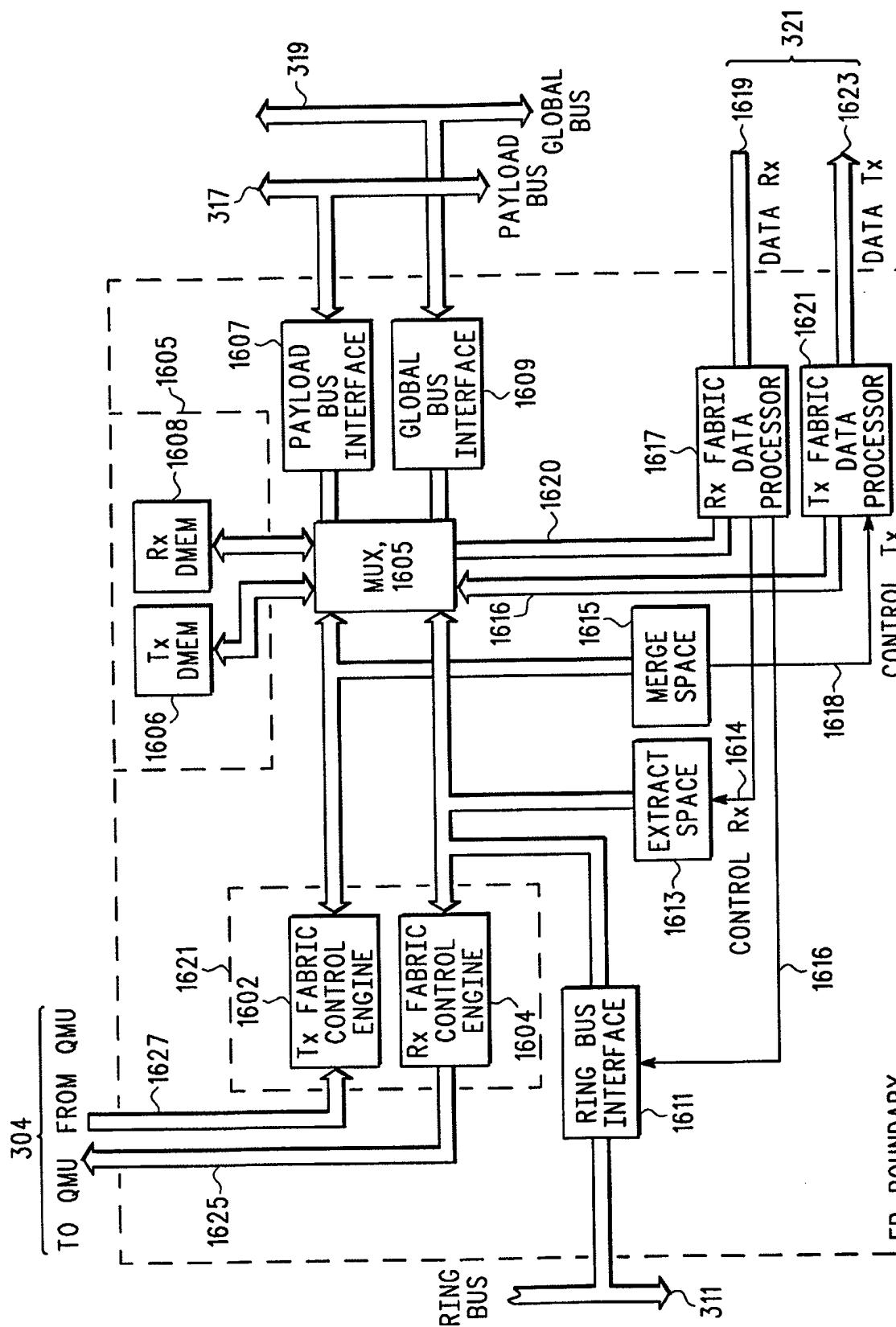


Fig. 16

303

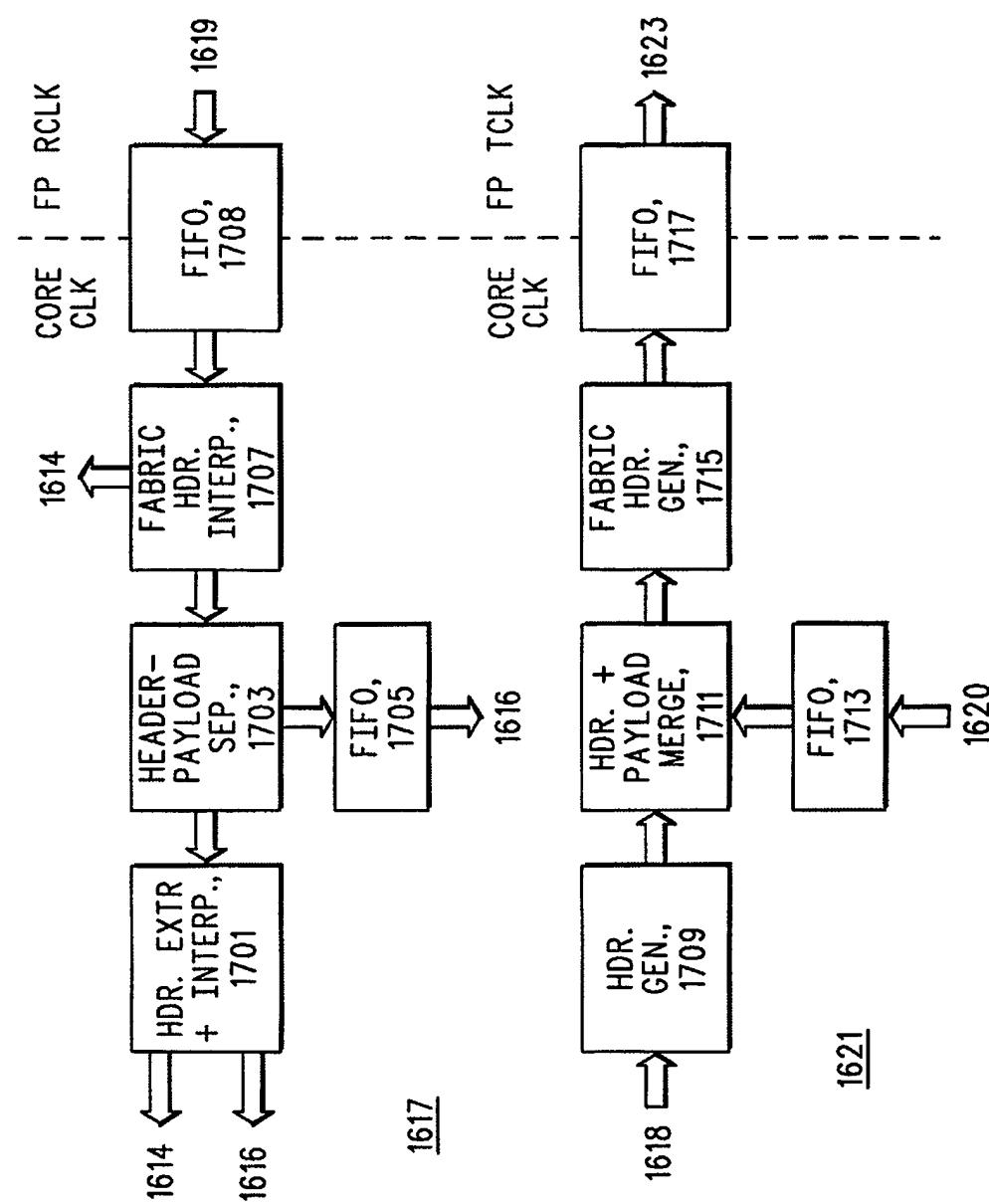


Fig. 17

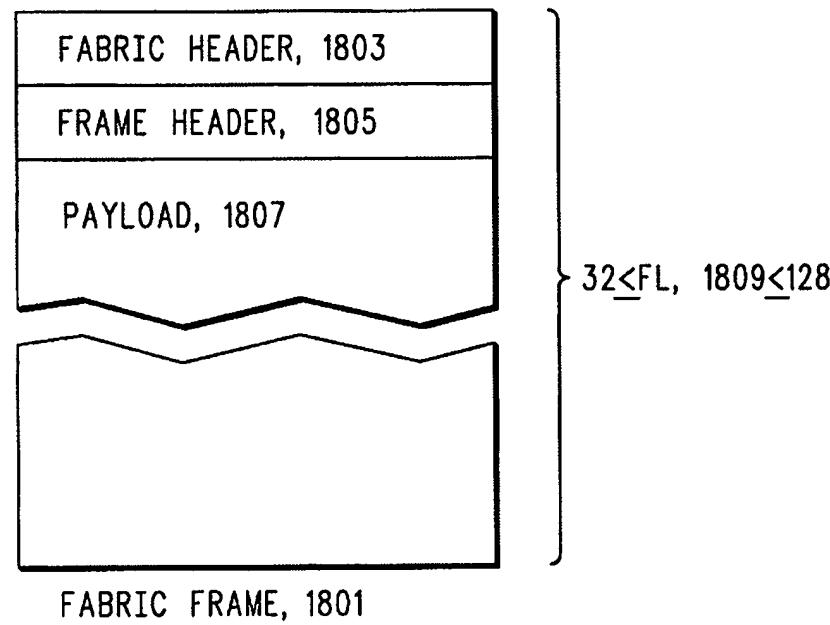


Fig. 18

L

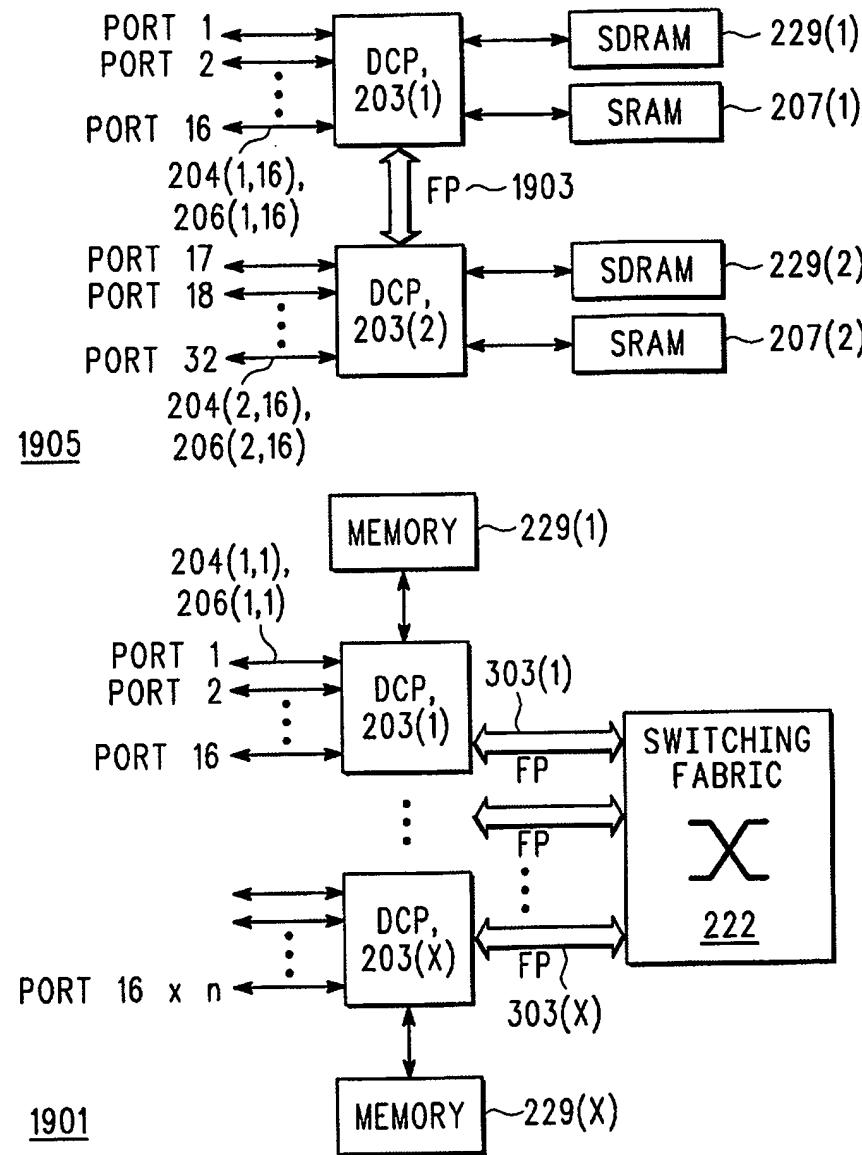
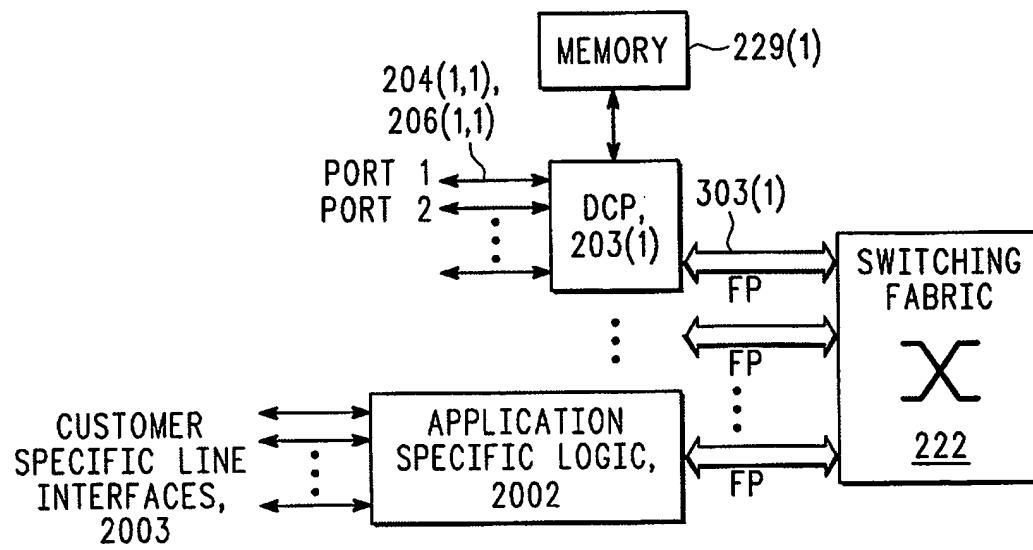


Fig. 19



2001

Fig. 20

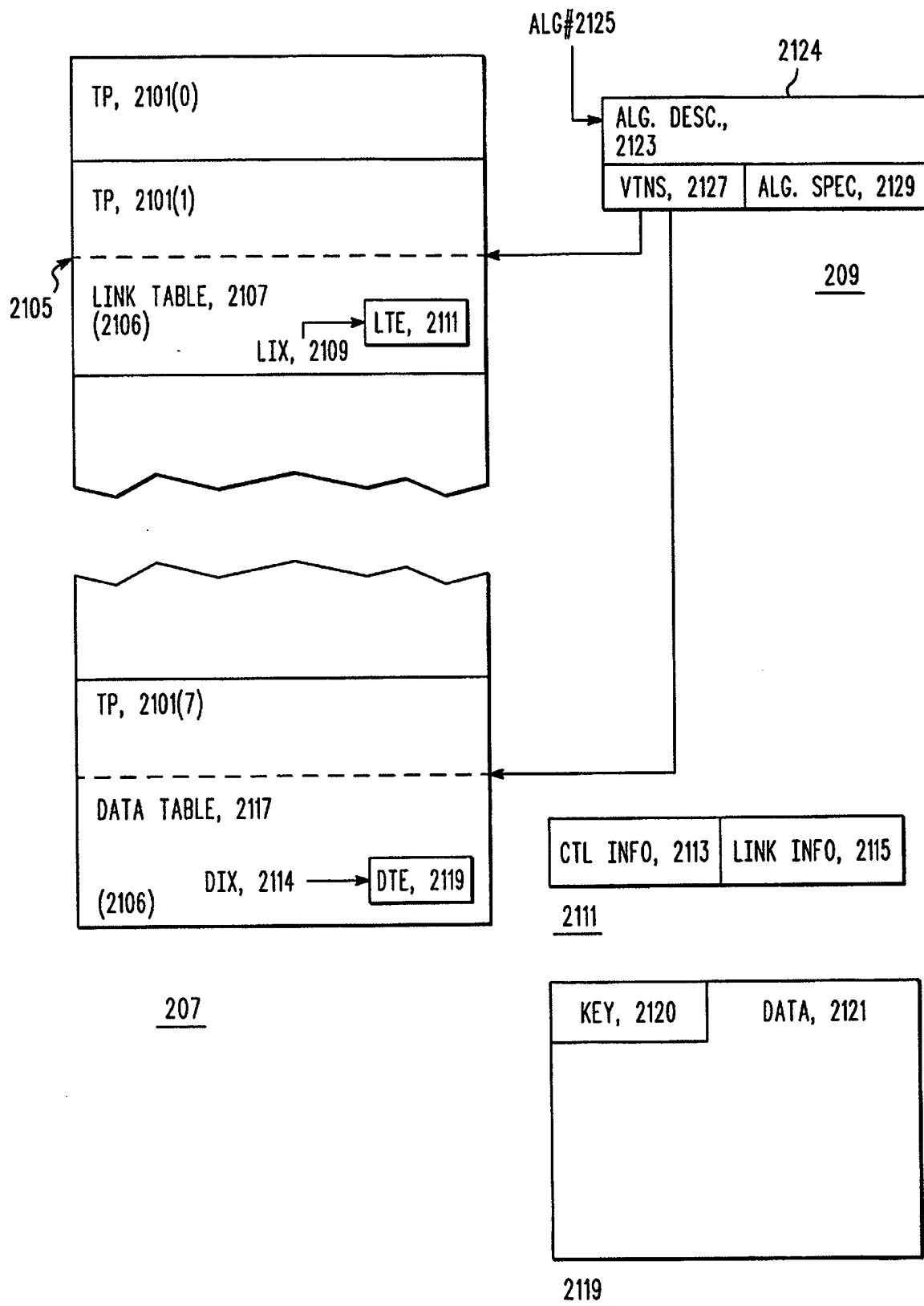


Fig. 21

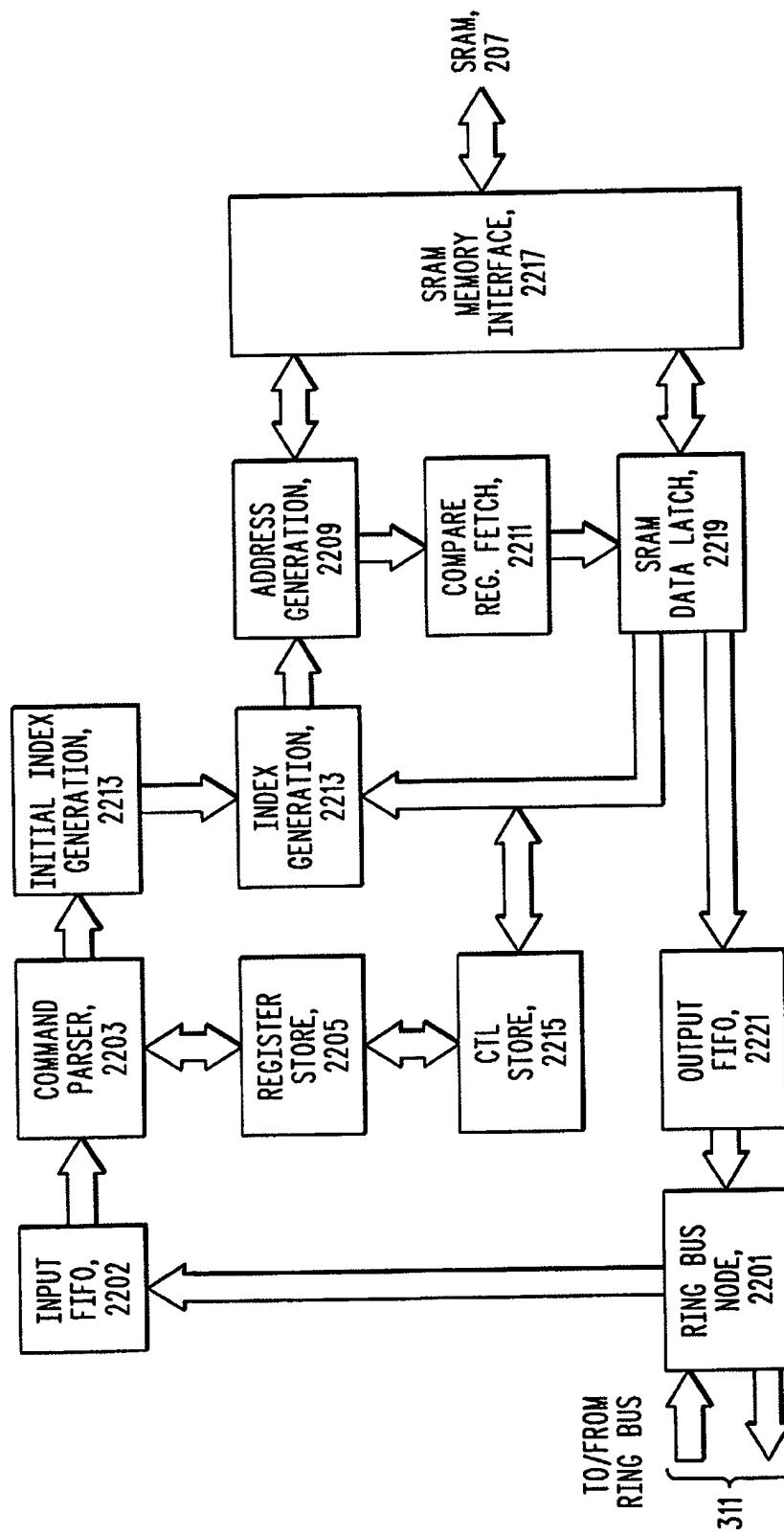


Fig. 22

301

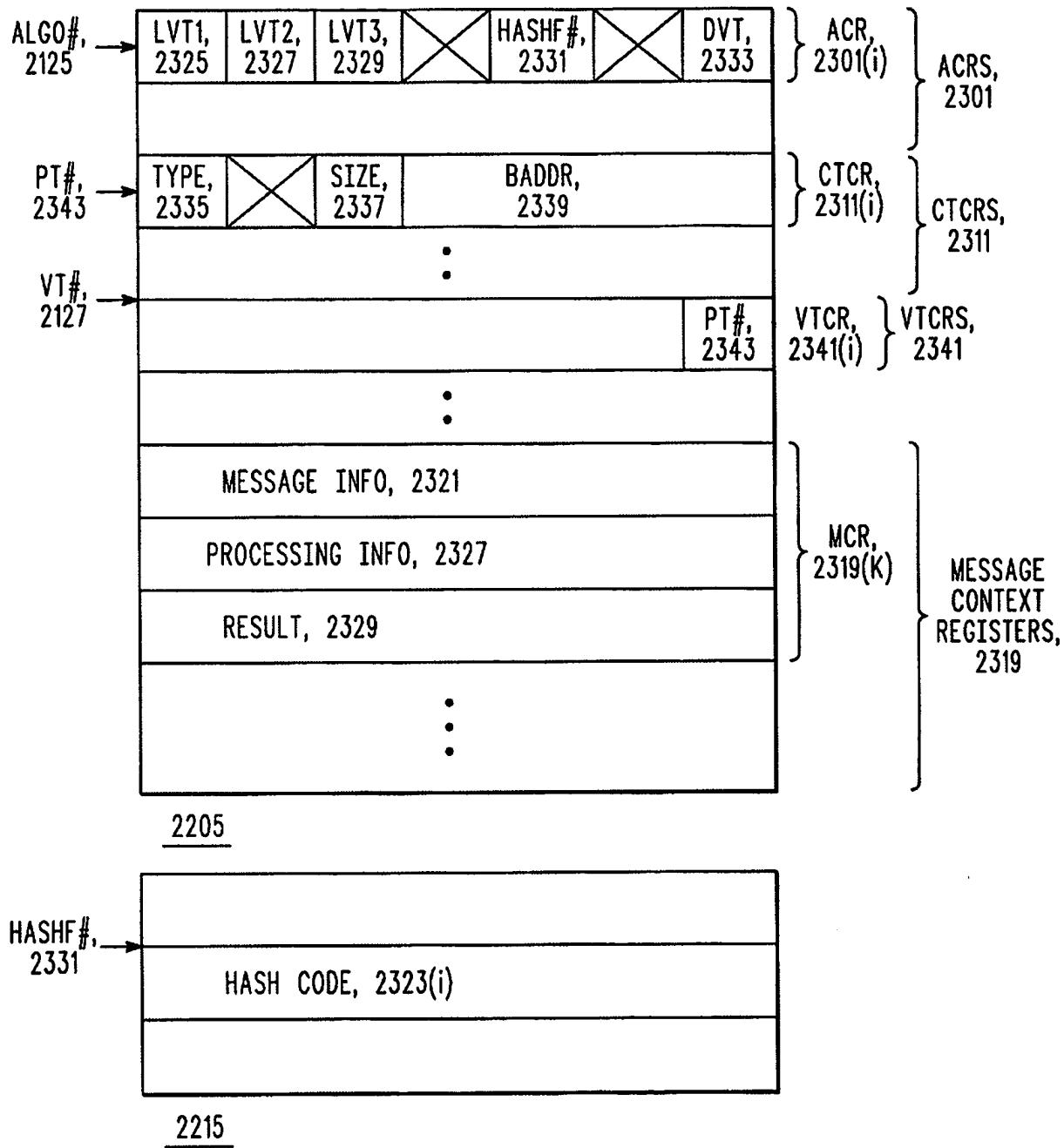


Fig. 23



# Replacement Sheet

BRIGHTMAN ET AL.  
SCI0981TS

24/47

COMMAND	COMMAND ID	RETURN DATA	DESCRIPTION
2421 { WRITE(VTABLE#,INDEX, MASK,DATA,OFFSET, LENGTH)	0X2	NONE	WRITE DATA INTO A VIRTUAL TABLE AT INDEX.
READ(VTABLE#,INDEX, OFFSET,LENGTH)	0X3	DATA	READS DATA FROM A VIRTUAL TABLE.
FINDW(ALG#,KEY)	0X6	PHYSICAL TABLE, INDEX, ERROR	FINDS A KEY USING ALG#. SETS RING BUS ERROR FLAG IF KEY IS NOT FOUND.
2423 { FINDW(ALG#,KEY,DATA, OFFSET,LENGTH)	0X4	PASS/FAIL, INDEX, ERROR	WRITES DATA INTO A TABLE USING A KEY. SETS RING BUS ERROR FLAG IF THE KEY IS NOT FOUND.
FINDR(ALG#,KEY,DATA, OFFSET,LENGTH)	0X5	PASS/FAIL, INDEX, DATA	READS LENGTH DWORDS OF DATA FROM A VTABLE# USING A KEY AT OFFSET DWORDS. SETS RING BUS ERROR FLAG IF THE KEY IS NOT FOUND
2425 { XOR(VTABLE#,INDEX, DATA/PCRC,OFFSET, MASK,CRC,LAST)	0X1	NONE OR CRC IN CRC MODE	XOR'S UP TO A 32 BIT VALUE TO OFFSET. ONLY MASKS OF UP TO FOUR CONSECUTIVE BYTES ARE VALID. A SPECIAL MODE EXISTS FOR CRC CALCULATIONS.
ADD(VTABLE#,INDEX, DATA,OFFSET,MASK)	0X7	NONE	ADDS UP TO A 32-BIT VALUE TO OFFSET. ONLY MASKS OF UP TO FOUR CONSECUTIVE BYTES ARE VALID.
2427 { WRITEREG(REG-ADDR, DATA)	0X0,0x10	NONE	WRITE DATA TO TLE REGISTER AT REG_ADDR.
READREG(REG_ADDR, DATA)	0X0,0x11	DATA	READ DATA FROM TLE REGISTER AT REG_ADDR.
ECHO(DATA)	0X0,0x04	DATA	RETURN DATA FROM TLE FOR TEST PURPOSES
NOP()	0X0,0x05	NONE	INSERTS A NOP INTO THE TLE PIPE

Fig. 24



# Replacement Sheet

OKIOMITAN ET AL.  
SCI0981TS

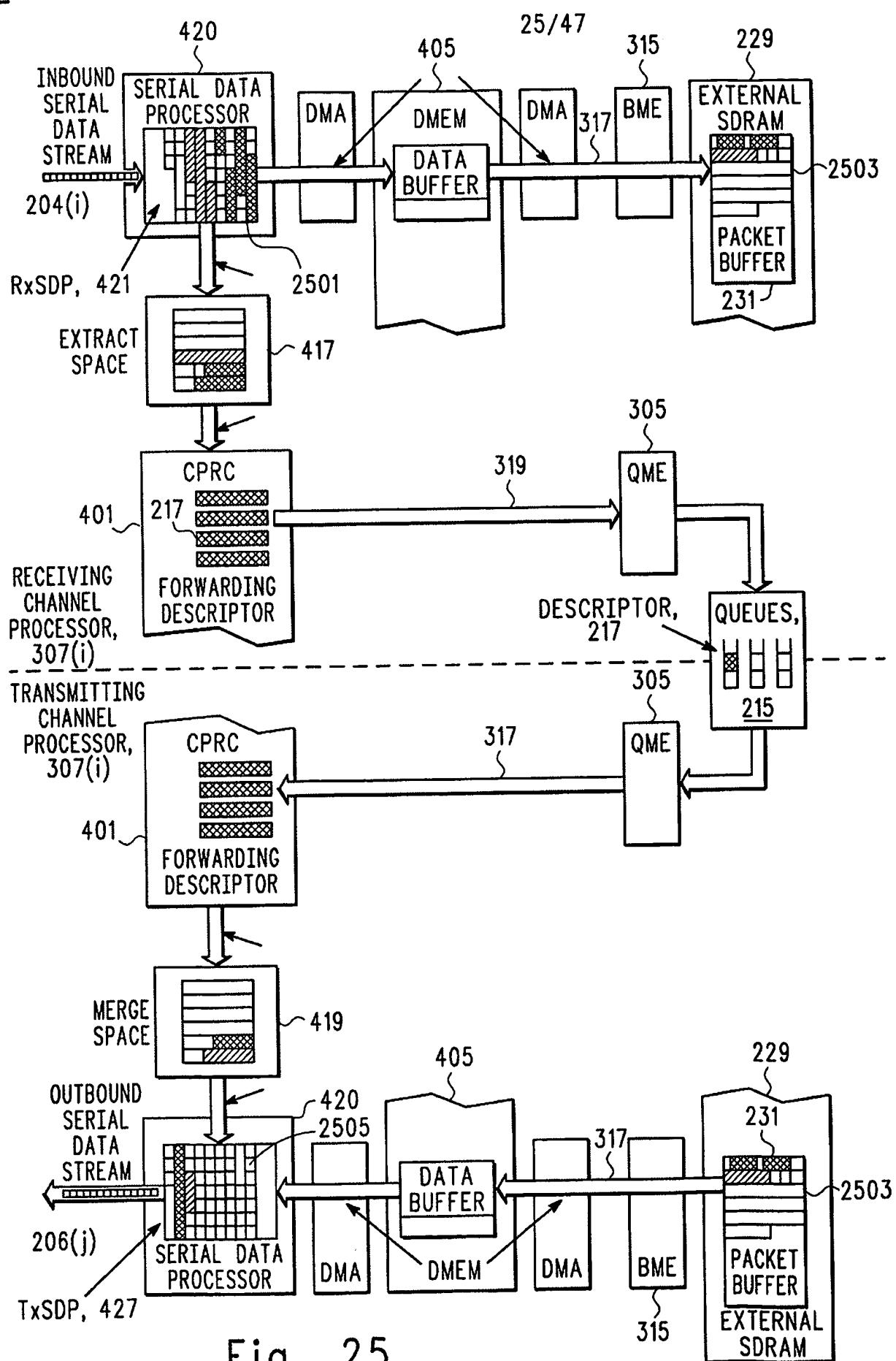
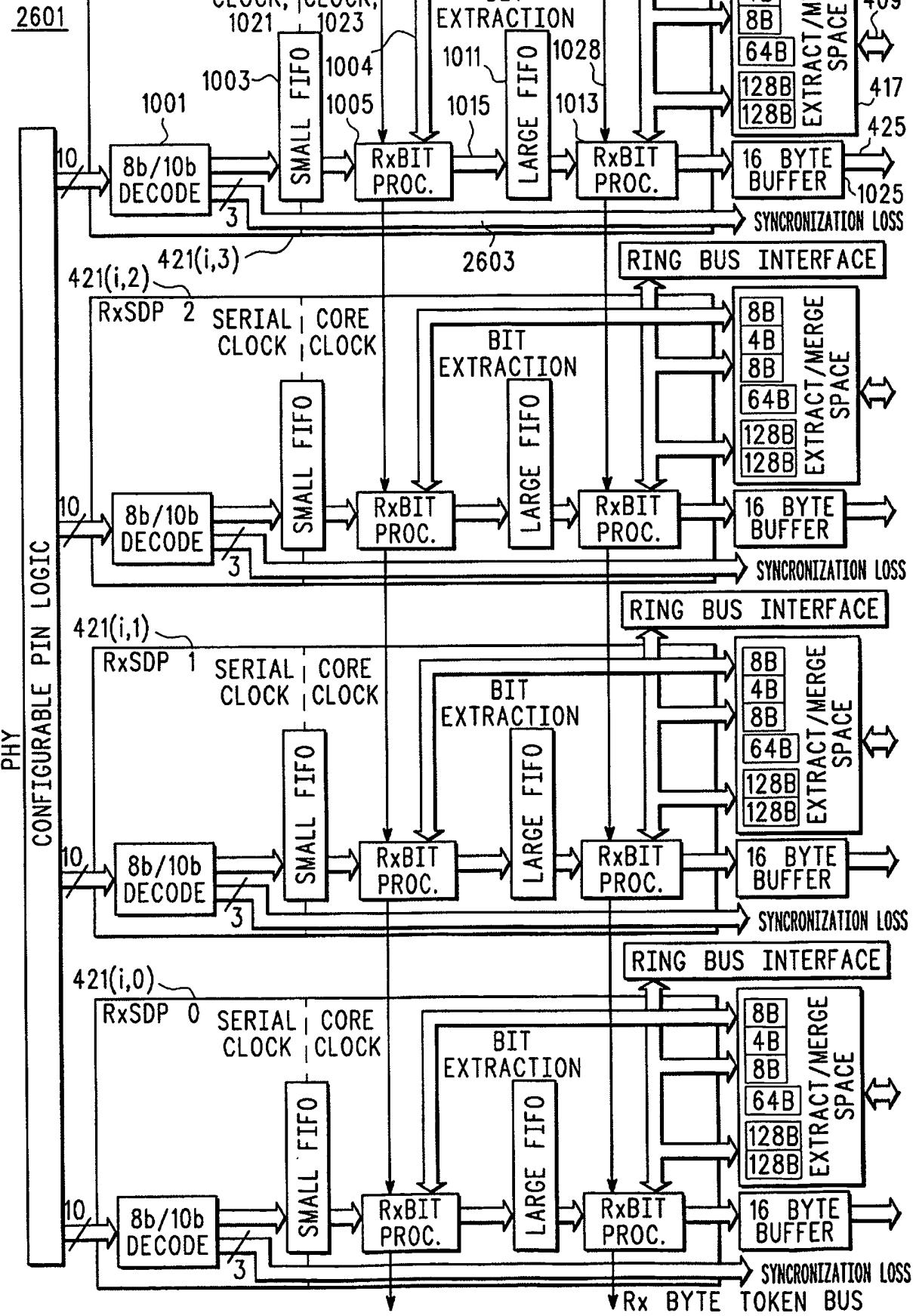


Fig. 25



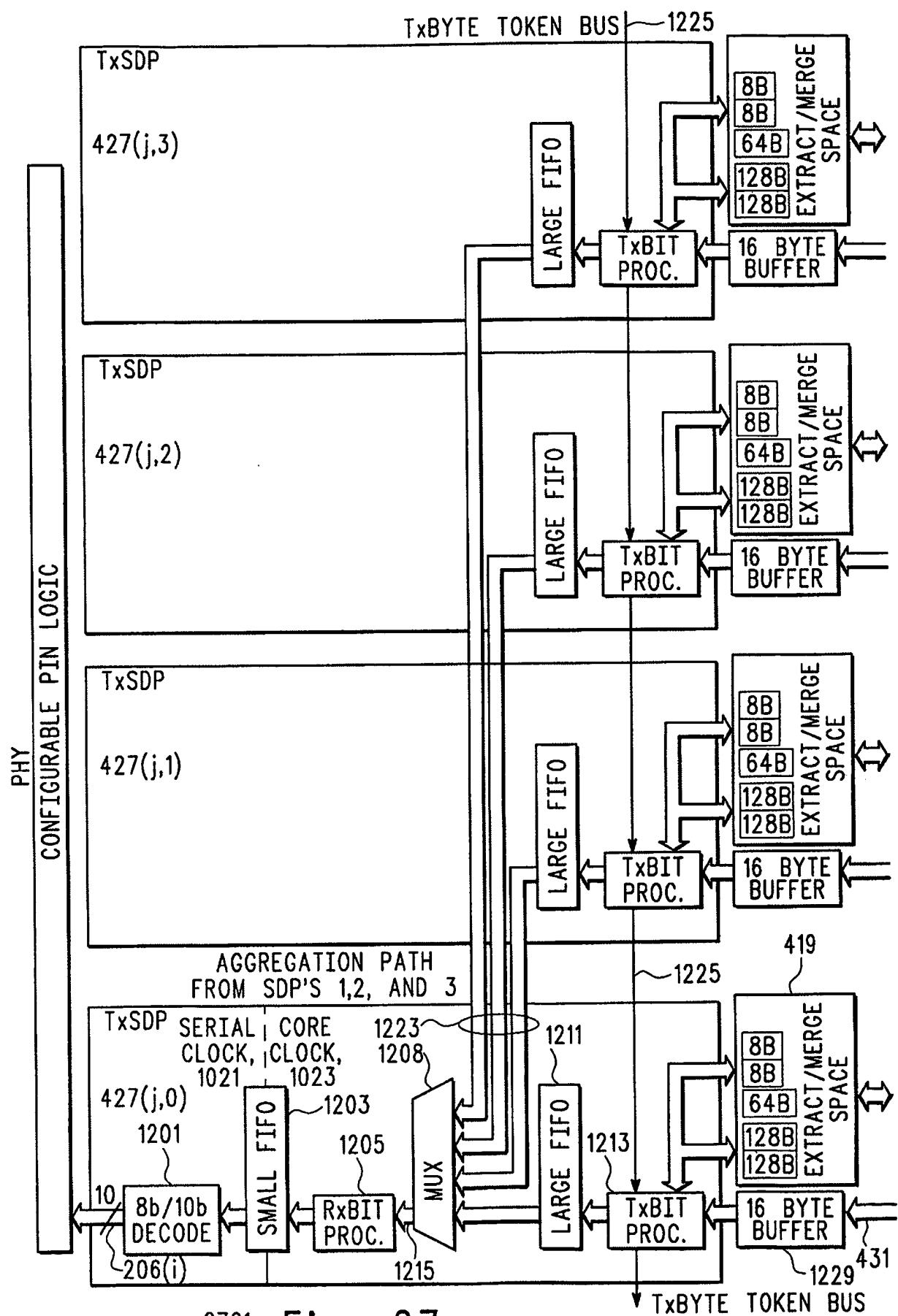
Fig. 26 1027 ~ RxBIT TOKEN BUS 26/47 RING BUS INTERFACE

2601





27/47



2701 Fig. 27

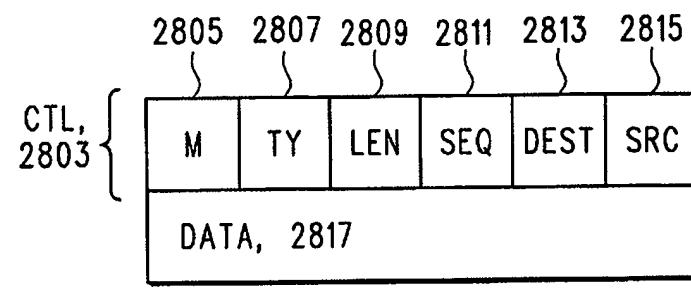


# Replacement Sheet

BRIJGMILAN ET AL.  
SCI0981TS

Γ

28/47



RING BUS MESSAGE, 2801

Fig. 28

└



Γ

29/47

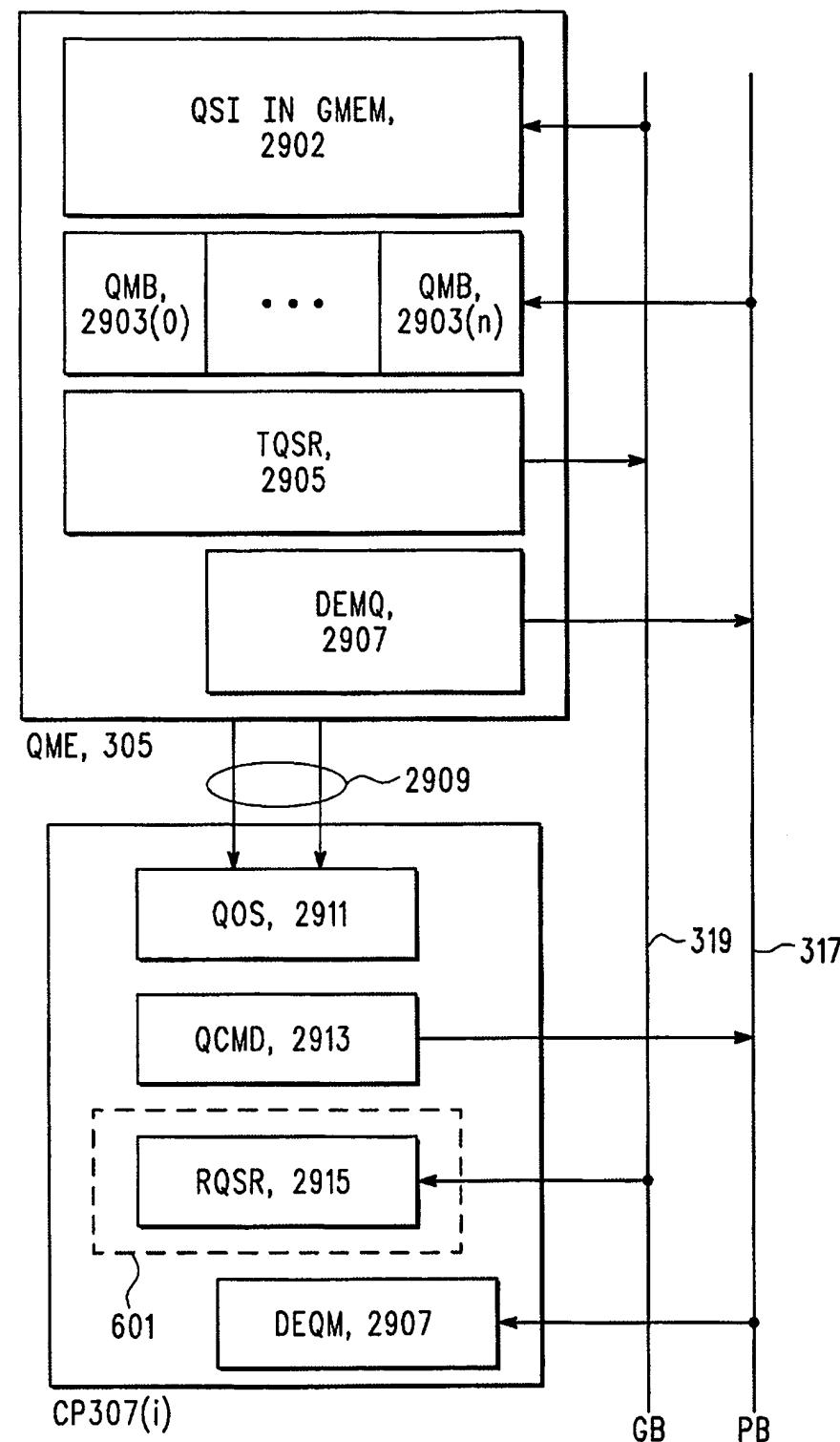
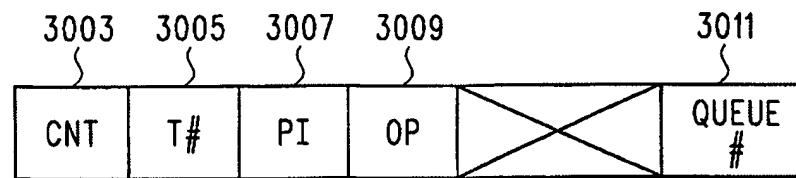
2901

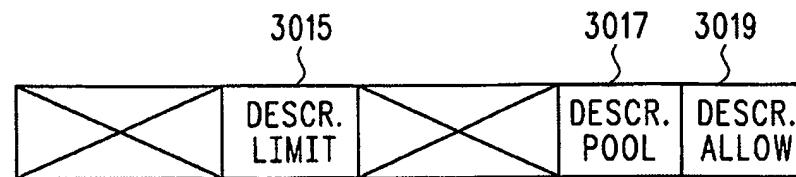
Fig. 29



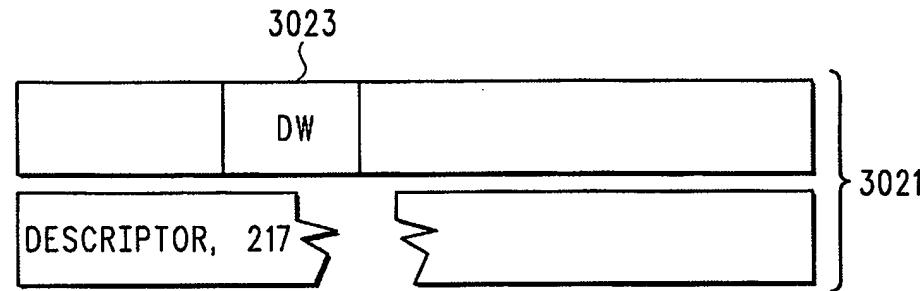
30/47



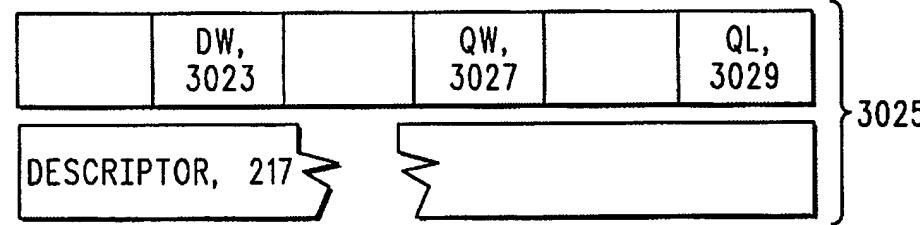
QUEUE INST. ADDR., 3001



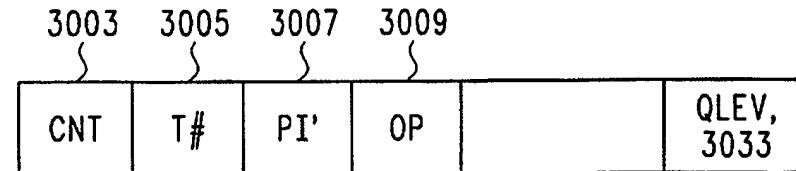
CONFIGURE QUEUE WRITE DATA., 3013



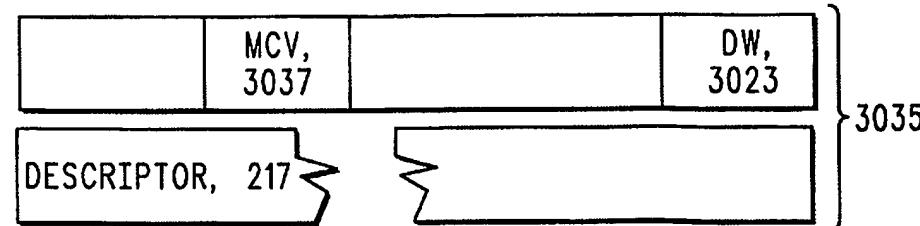
UNICAST ENQUEUE DATA



UNICAST DEQUEUE DATA



MULTICAST ENQUEUE INST. ADDR., 3031



MULTICAST ENQUEUE DATA

2913

Fig. 30



# Replacement Sheet

DRUMMIE ET AL.  
SCI0981TS

31/47

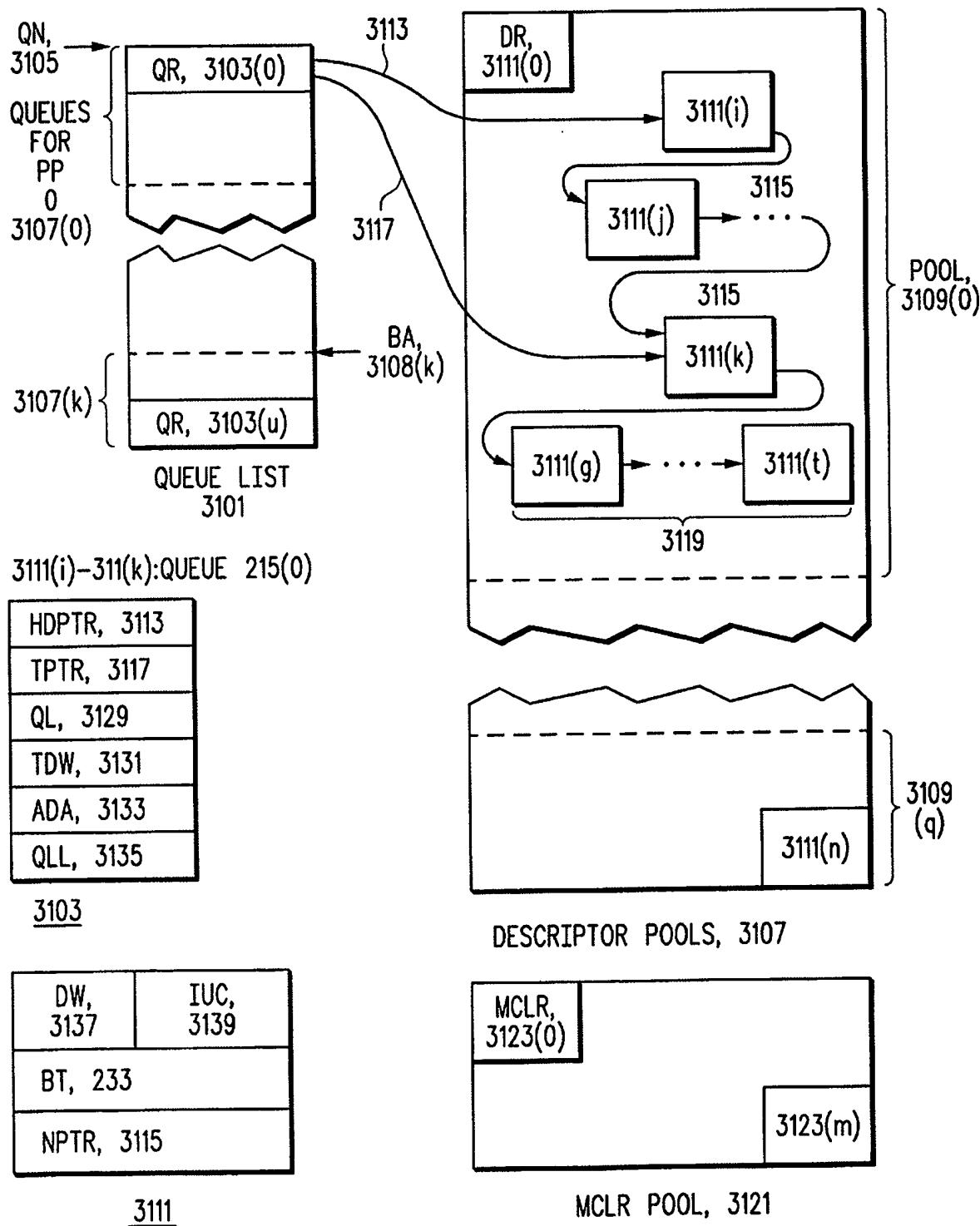
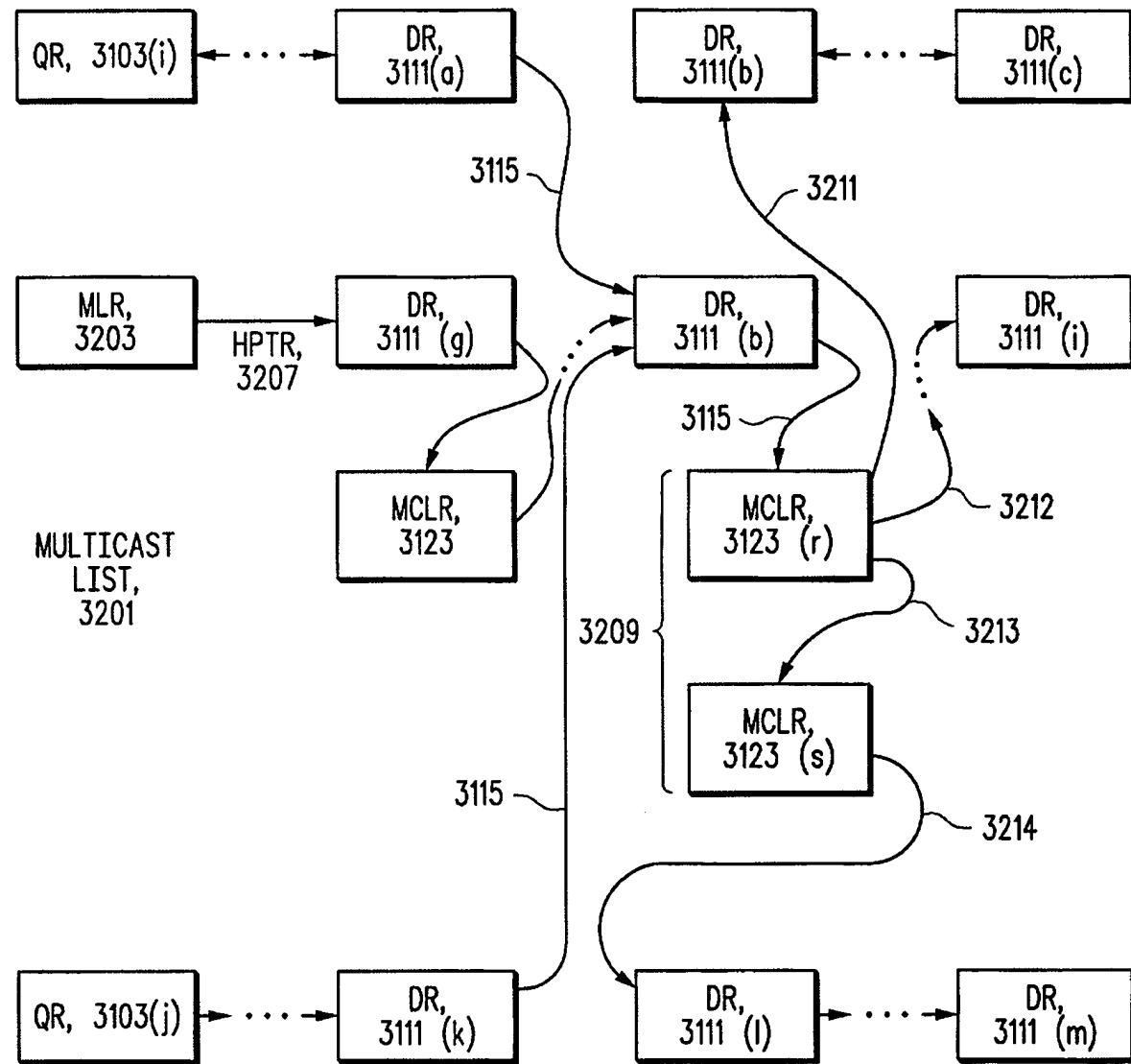


Fig. 31



UNICAST QUEUE, 215(i)



UNICAST QUEUE, 215(j)

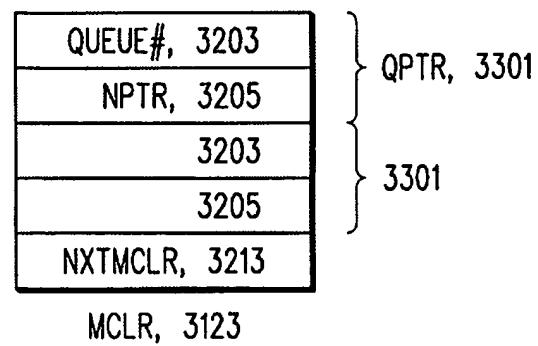
Fig. 32



# Replacement Sheet

BRIJNARAYAN ET AL.  
SCI098ITS

33/47



USER #, QUEUING LEVEL#3309

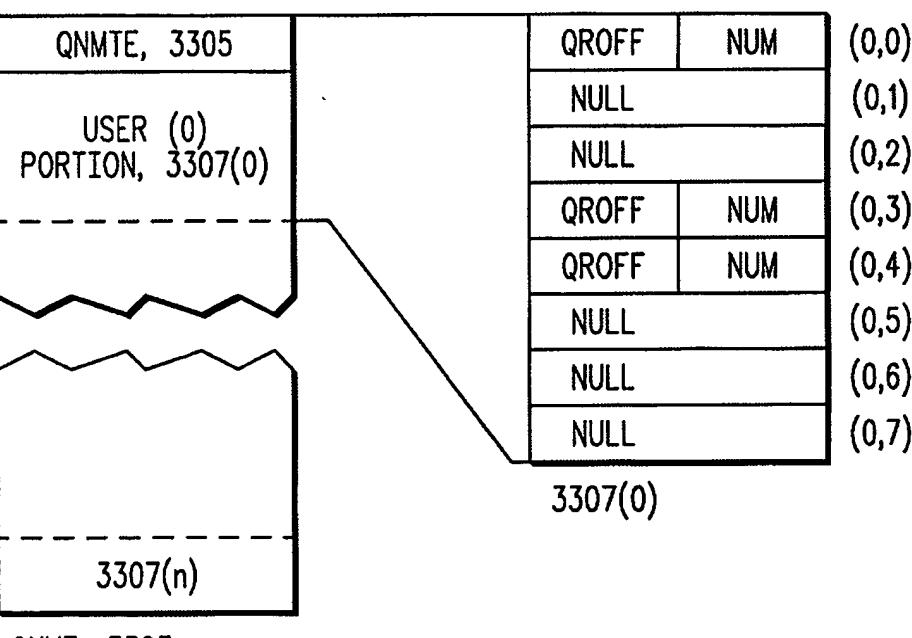


Fig. 33

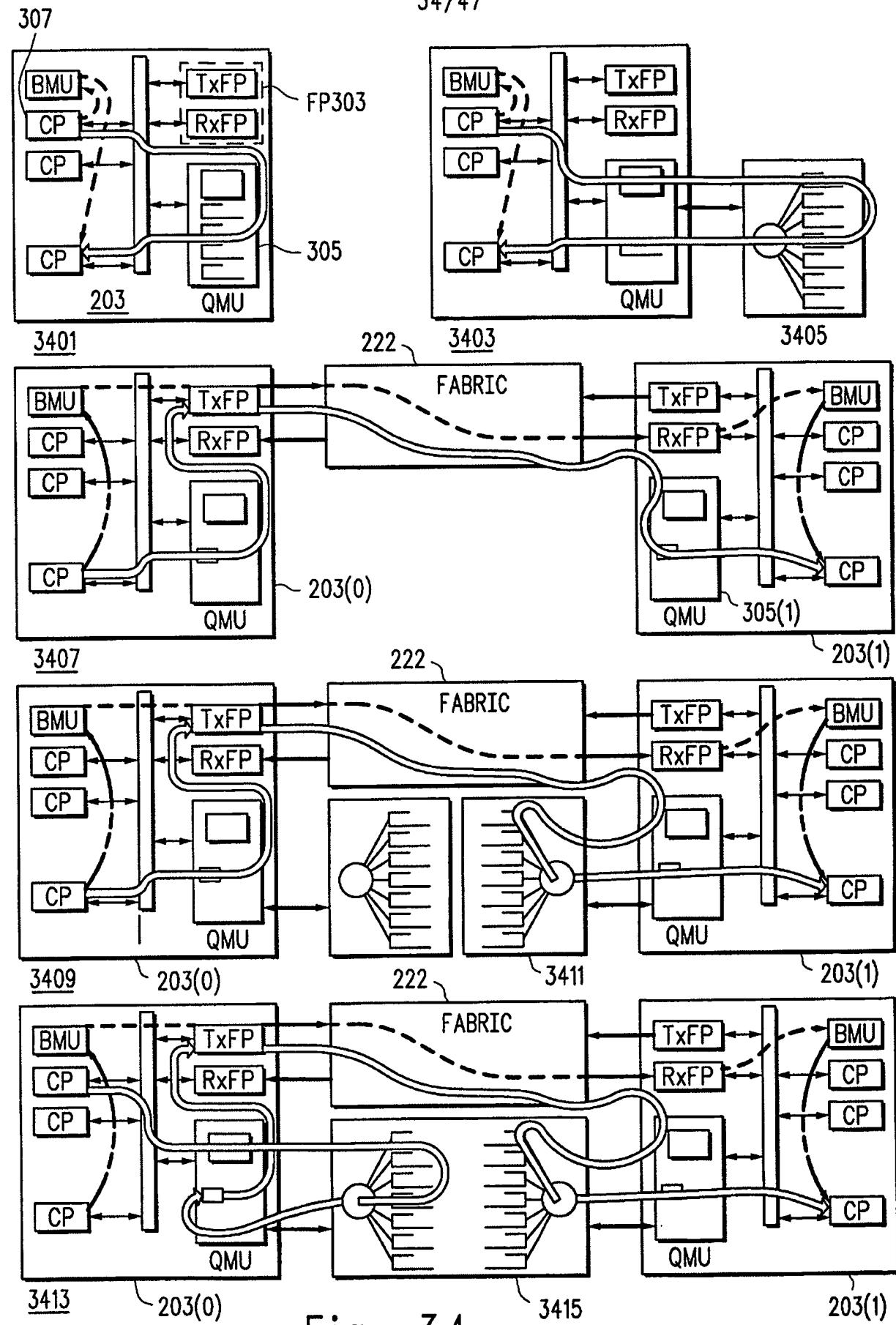


Fig. 34



35/47

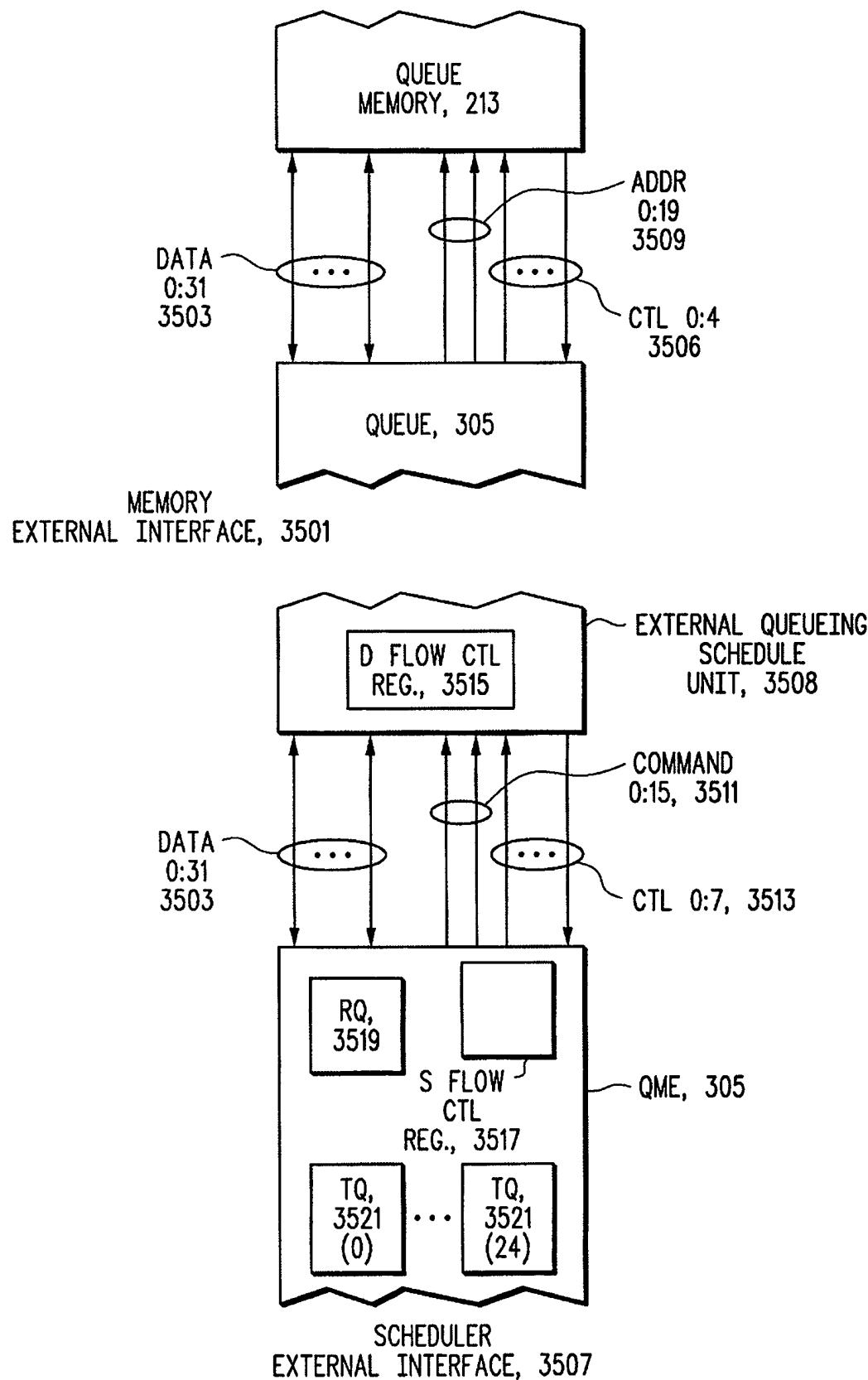


Fig. 35

J

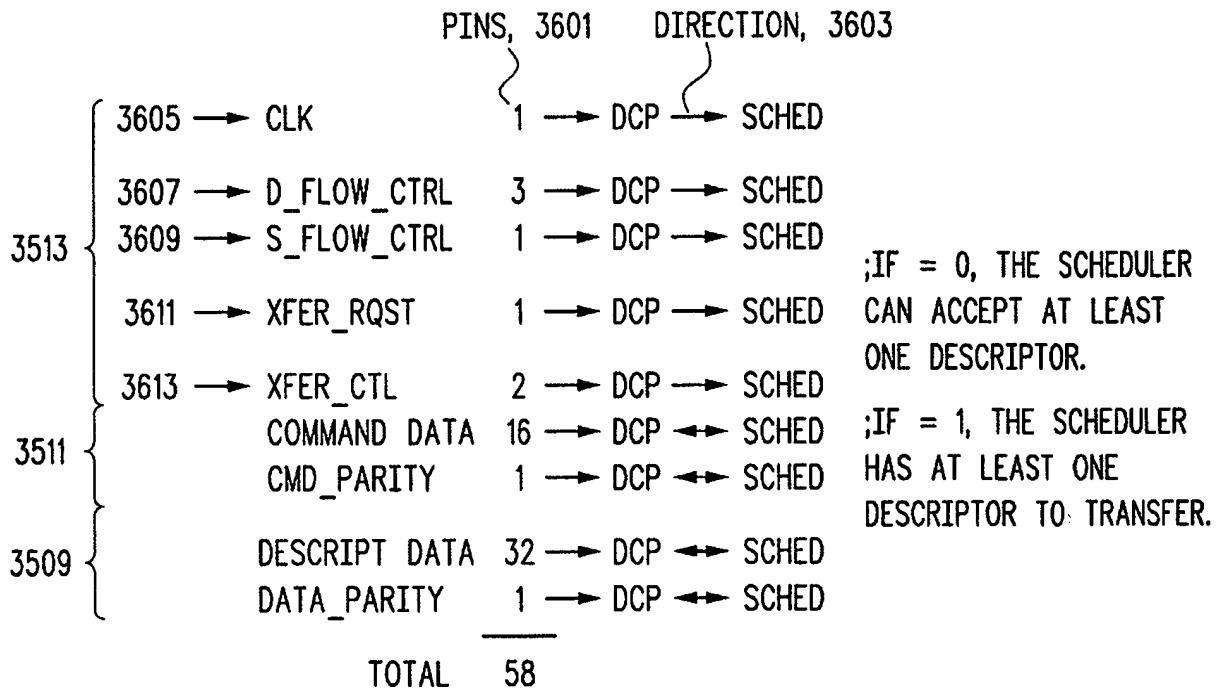
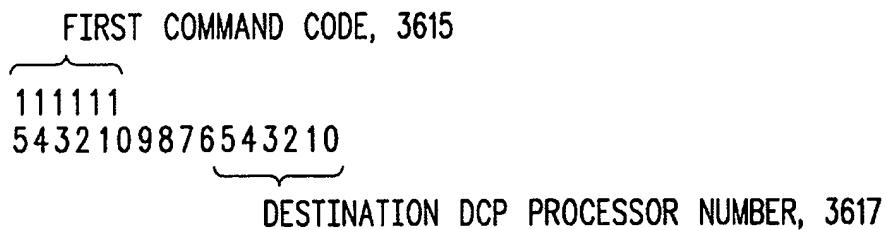
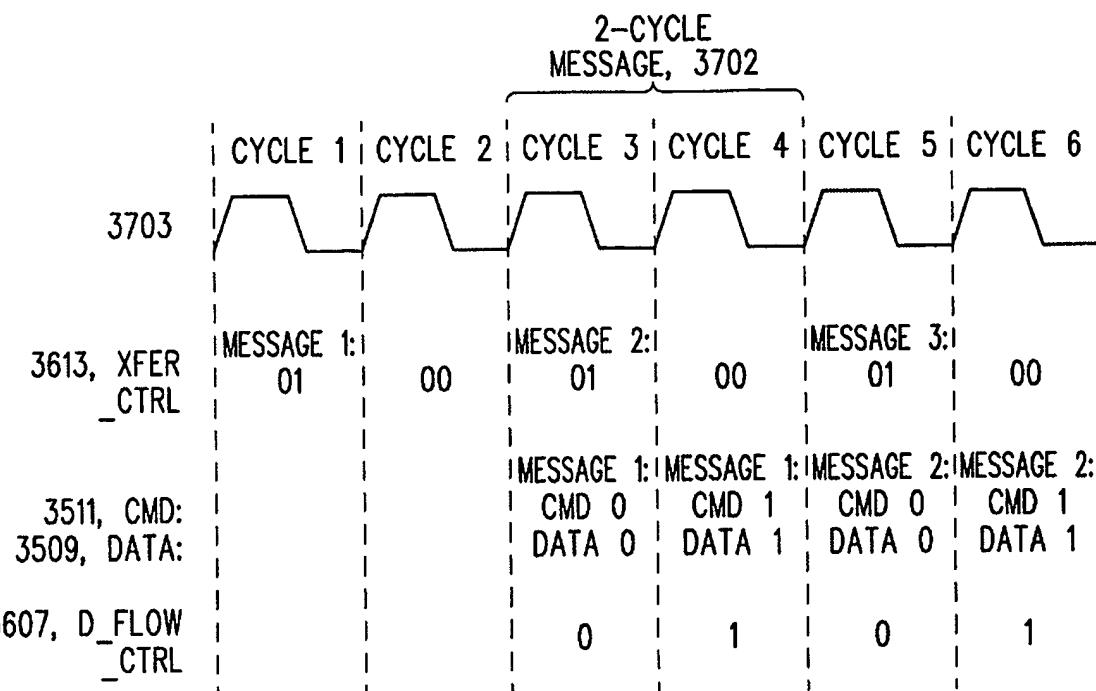
35073514

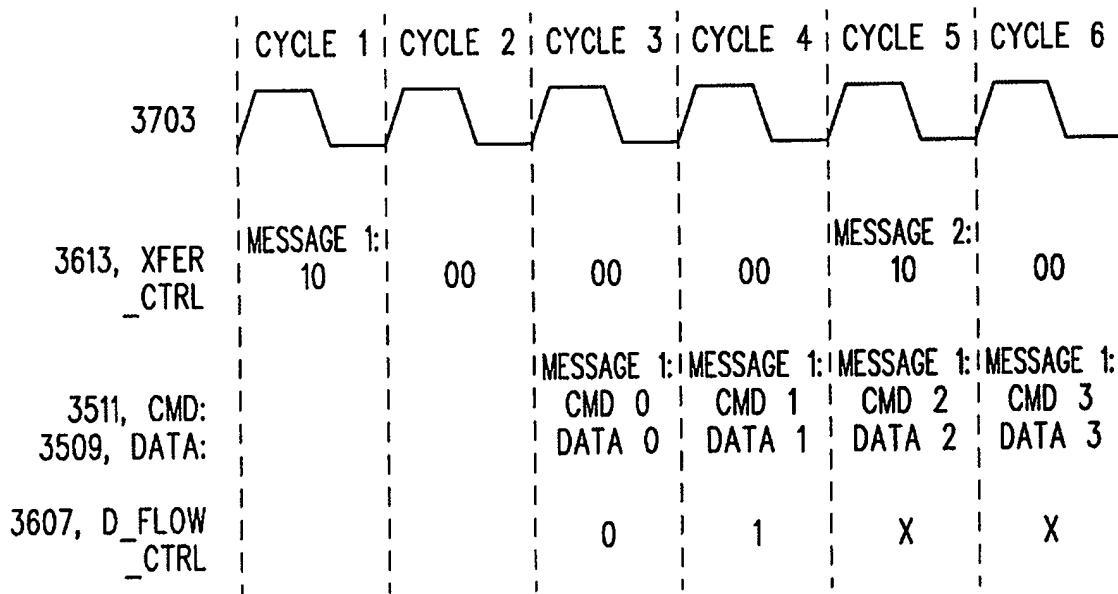
Fig. 36



37/47

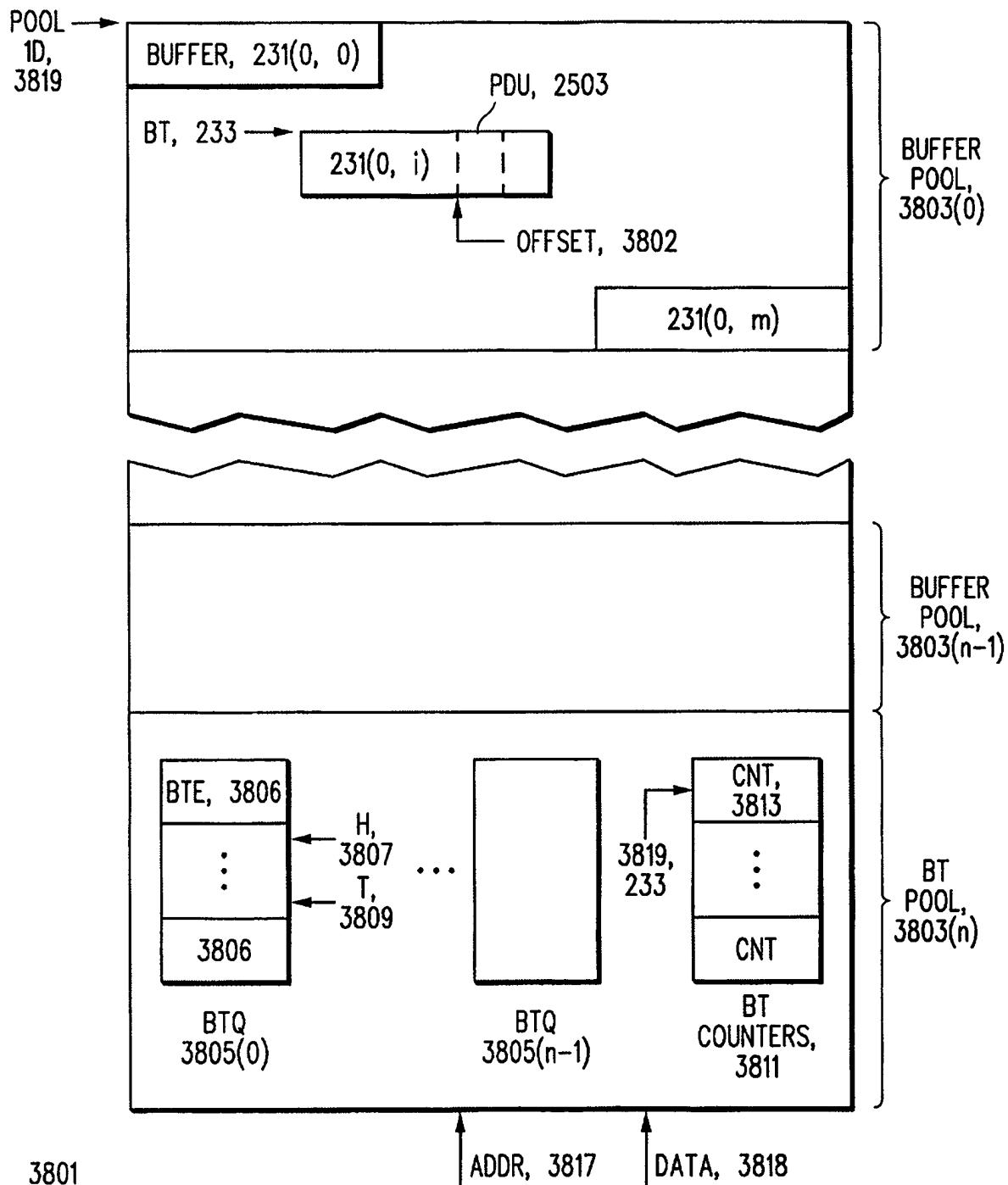


3701: 2 2-CYCLE MESSAGES



3705: 2-4 CYCLE MESSAGES

4-CYCLE  
MESSAGE, 3702



PB,  
317

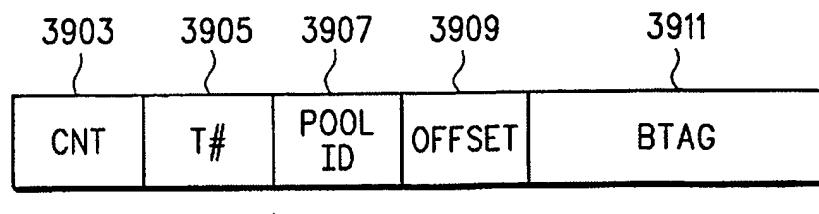
Fig. 38



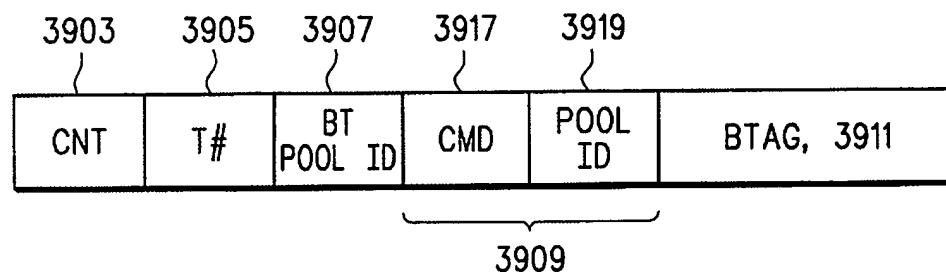
# Replacement Sheet

OKLOOMIAN ET AL.  
SCI098ITS

39/47



PAYLOAD BUS  
BUFFER READ/WRITE COMMAND, 3901



PAYLOAD BUS BTAG - COMMAND, 3915

Fig. 39

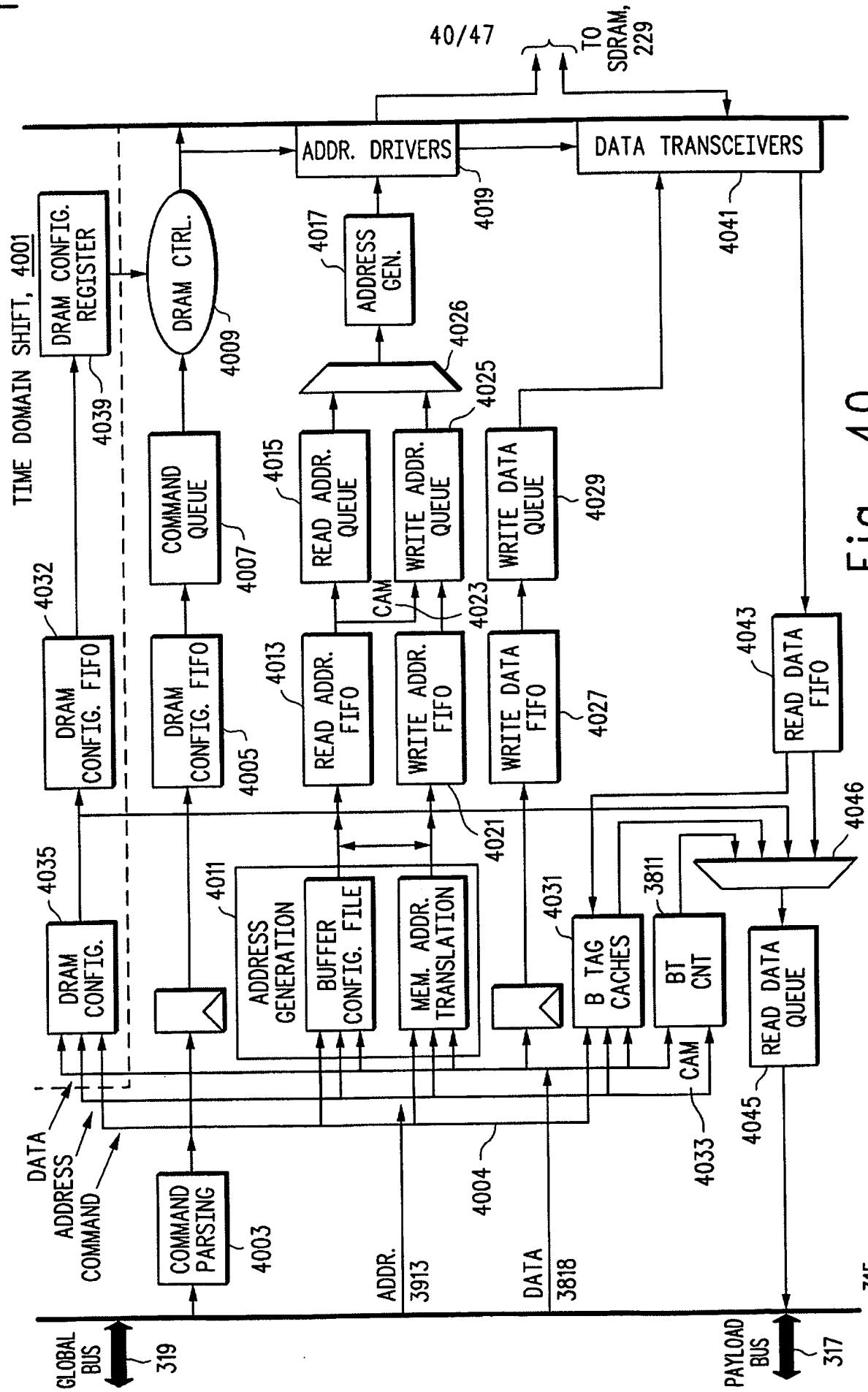


Fig. 40

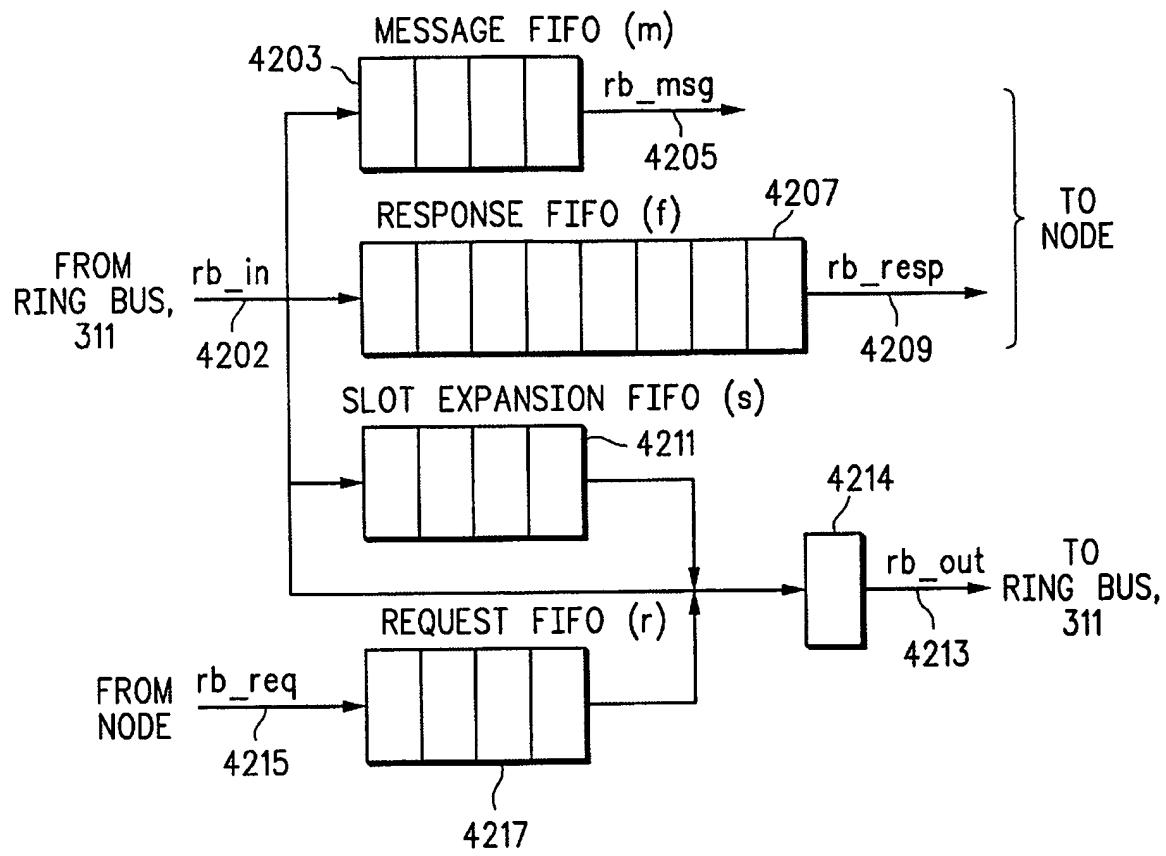


41/47

RTOS, 4101
BTAG AND BUFFER POOLS, 4103
-----
XP DATA MEMORY, 4105
TRANSLATION TABLES, 4107
PACKET PROCESSOR CODE AND DATA, 4109
MEMORY CONFIG. INFO, 4111

229

Fig. 41



RING BUS  
NODE INTERFACE, 4201

Fig. 42

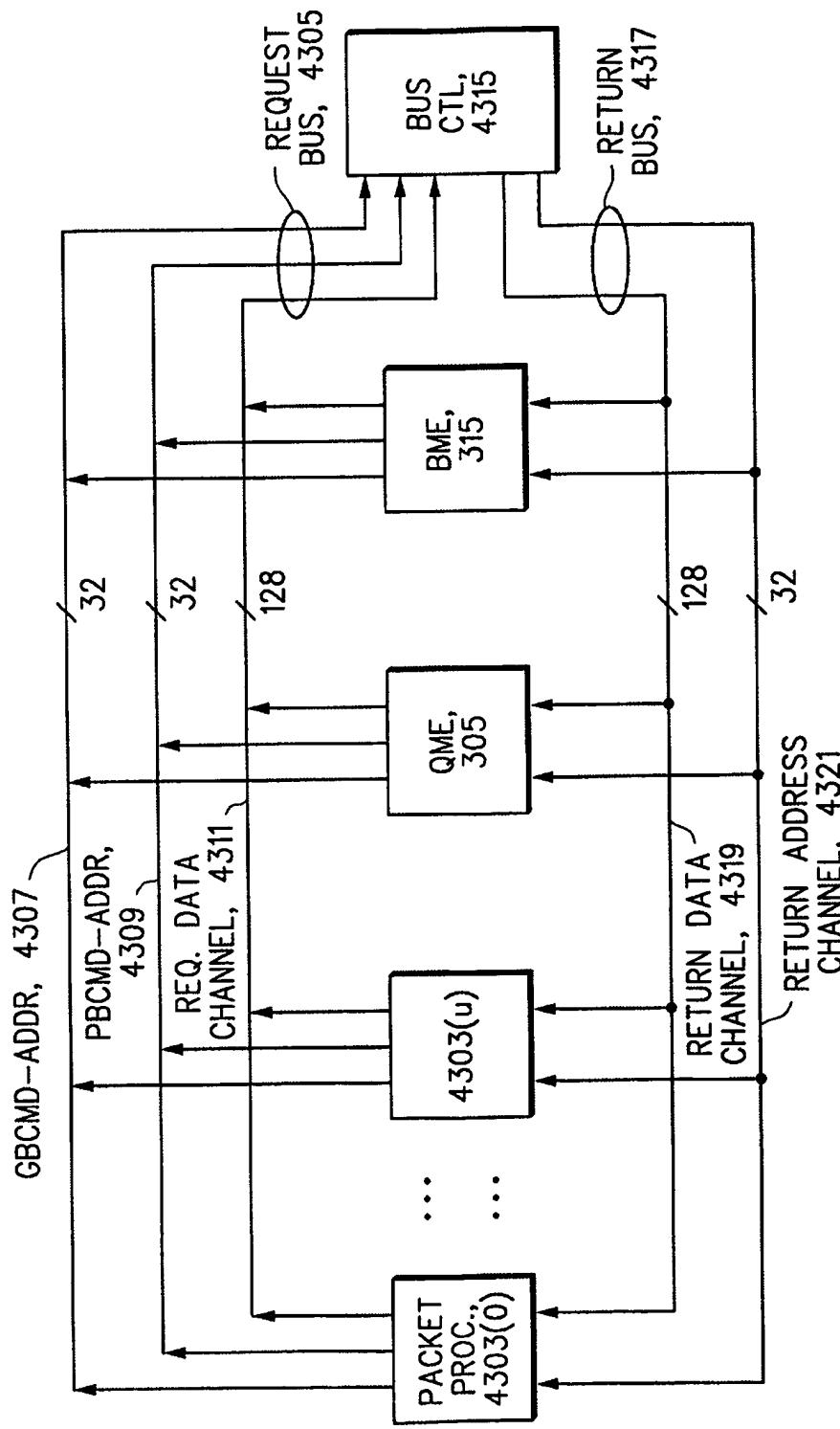


Fig. 43

4301

L





45/47

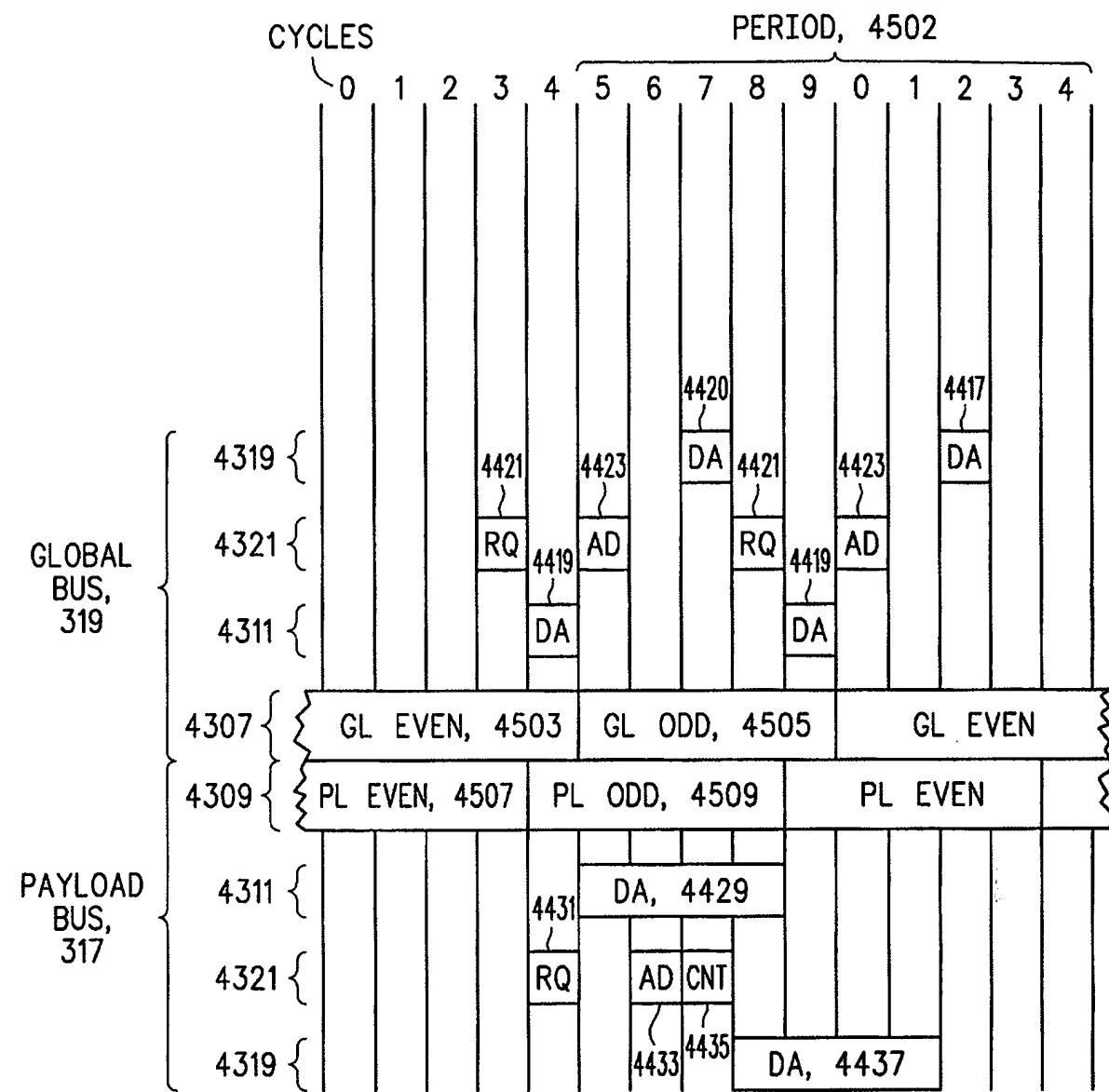
4501

Fig. 45

## Replacement Sheet

BRIGHTMAN ET AL.  
SCI0981TS

46/47

PIN	PURPOSE	RMII	OC-3	DS1	DS3	GMII (Tx)	GMII (Rx)	TBI (Tx)	TBI (Rx)	OC-12
CP0_0	OUTCLK	REF_CLK	RCLK_H	TCLK	TCLK	TCLK	nc	TCLK	nc	TCLK
_1	INCLK	CRS_DV	RCLK_L	RCLK	RCLK	CRS	nc		nc	TCLK1
_2	DATA	TXD(0)	TXD_H	TDATA	TDATA	TXD(0)	nc	TXD(0)	nc	TDX(0)
_3	DATA	TXD(1)	TXD_L	TxFRAME	TxFRAME	TXD(1)	nc	TXD(1)	nc	TDX(1)
_4	DATA	RXD(0)	RXD_H	RDATA	RDATA	TXD(2)	nc	TXD(2)	nc	TDX(2)
_5	DATA	RXD(1)	RXD_L	RxFRAME	RxFRAME	TXD(3)	nc	TXD(3)	nc	TDX(3)
_6	DATA	TX-EN	SIGNAL_DET			TX_EN	nc	TXD(4)	nc	
CP1_0	OUTCLK	REF_CLK	RCLK_H	TCLK	TCLK					
_1	INCLK	CRS_DV	RCLK_L	RCLK	RCLK	COL	nc			
_2	DATA	TXD(0)	TXD_H	TDATA	TDATA	TXD(4)	nc	TXD(5)	nc	TDX(4)
_3	DATA	TXD(1)	TXD_L	TxFRAME	TxFRAME	TXD(5)	nc	TXD(6)	nc	TDX(5)
_4	DATA	RXD(0)	RXD_H	RDATA	RDATA	TXD(6)	nc	TXD(7)	nc	TDX(6)
_5	DATA	RXD(1)	RXD_L	RxFRAME	RxFRAME	TXD(7)	nc	TXD(8)	nc	TDX(7)
_6	DATA	TX-EN	SIGNAL_DET			TX_ER	nc	TXD(9)	nc	
CP2_0	OUTCLK	REF_CLK	RCLK_H	TCLK	TCLK					
_1	INCLK	CRS_DV	RCLK_L	RCLK	RCLK	nc	RCLX	nc	RCLK	RCLK1
_2	DATA	TXD(0)	TXD_H	TDATA	TDATA	nc	RXD(0)	nc	RXD(1)	RDX(0)
_3	DATA	TXD(1)	TXD_L	TxFRAME	TxFRAME	nc	RXD(1)	nc	RXD(0)	RDX(1)
_4	DATA	RXD(0)	RXD_H	RDATA	RDATA	nc	RXD(2)	nc	RXD(2)	RDX(2)
_5	DATA	RXD(1)	RXD_L	RxFRAME	RxFRAME	nc	RXD(3)	nc	RXD(3)	RDX(3)
_6	DATA	TX-EN	SIGNAL_DET			nc	RX_DV		RXD(8)	FP
CP3_0	OUTCLK	REF_CLK	RCLK_H	TCLK	TCLK					
_1	INCLK	CRS_DV	RCLK_L	RCLK	RCLK			nc	RCLKN	
_2	DATA	TXD(0)	TXD_H	TDATA	TDATA	nc	RXD(4)	nc	RXD(4)	RDX(4)
_3	DATA	TXD(1)	TXD_L	TxFRAME	TxFRAME	nc	RXD(5)	nc	RXD(5)	RDX(5)
_4	DATA	RXD(0)	RXD_H	RDATA	RDATA	nc	RXD(6)	nc	RXD(6)	RDX(6)
_5	DATA	RXD(1)	RXD_L	RxFRAME	RxFRAME	nc	RXD(7)	nc	RXD(7)	RDX(7)
_6	DATA	TX-EN	SIGNAL_DET			nc	RX_ER	nc	RXD(9)	LOCKDET

4601

Fig. 46

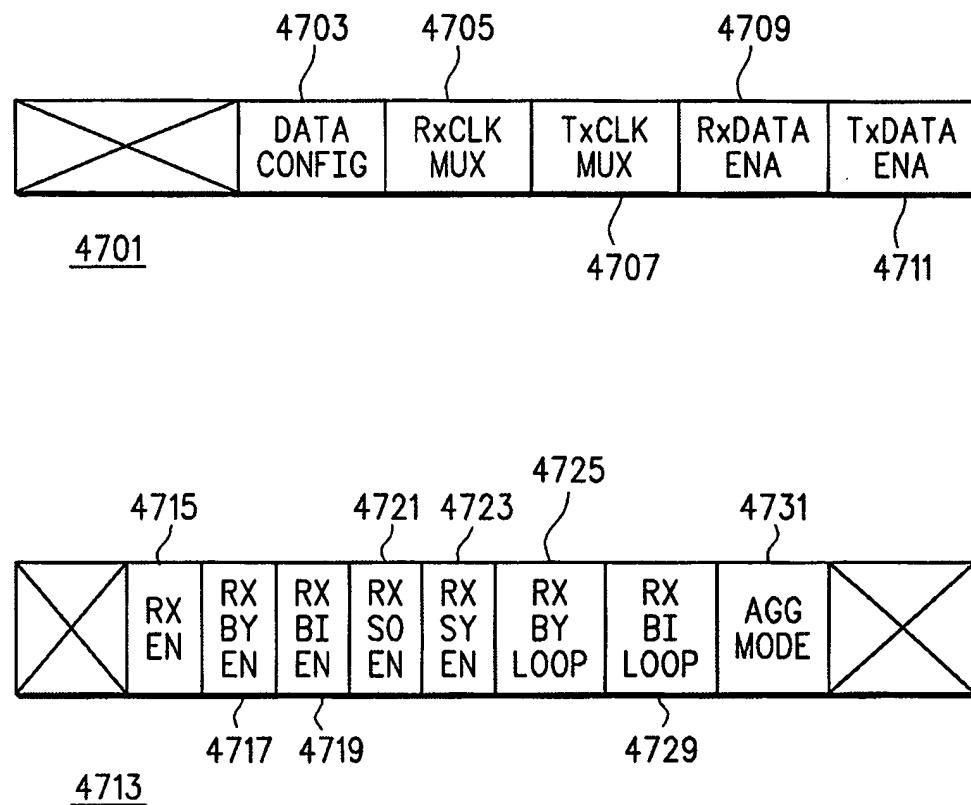


Fig. 47